

## Schematics Page Index (Title / Revision / Change Date)

Page	Title of Schematics Page	Rev.	Date	Page	Title of Schematics Page	Rev.	Date
01	Index page	1.0	07'10/19	36	Flash ROM/XBUS	1.0	07'10/19
02	Block Diagram	1.0	07'10/19	37	Mini-PCIE Card	1.0	07'10/19
03	Merom(HOST BUS) 1/3	1.0	07'10/19	38	FeliCa/MDC	1.0	07'10/19
04	Merom(HOST BUS) 2/3	1.0	07'10/19	39	EXPRESS	1.0	07'10/19
05	Merom(Power/Gnd) 3/3	1.0	07'10/19	40	AUDIO(CODEC/POWER) 1/4	1.0	07'10/19
06	CLOCK GEN	1.0	07'10/19	41	AUDIO( AMP/HP/SPK) 2/4	1.0	07'10/19
07	Crestline (HOST) 1/7	1.0	07'10/19	42	AUDIO( EXTMIC) 3/4	1.0	07'10/19
08	Crestline (DMI) 2/7	1.0	07'10/19	43	AUDIO(MUTE) 4/4	1.0	07'10/19
09	Crestline (GRAPHIC) 3/7	1.0	07'10/19	44	FAN/Thermal-Sensor	1.0	07'10/19
10	Crestline (DDRII) 4/7	1.0	07'10/19	45	PCI (PCI BUS) 1/3	1.0	07'10/19
11	Crestline (POWER,VCC) 5/7	1.0	07'10/19	46	PCI (i.LINK) 2/3	1.0	07'10/19
12	Crestline (VCC CORE) 6/7	1.0	07'10/19	47	PCI (SD/MS-DUO) 3/3	1.0	07'10/19
13	Crestline (VSS) 7/7	1.0	07'10/19	48	USB2.0	1.0	07'10/19
14	DDRII(SO-DIMM_0) 1/3	1.0	07'10/19	49	LAN (88E8039)	1.0	07'10/19
15	DDRII(SO-DIMM_1) 2/3	1.0	07'10/19	50	LAN Transformer	1.0	07'10/19
16	DDRII(Termination) 3/3	1.0	07'10/19	51	Touch/Lid/LED	1.0	07'10/19
17	VGA(PCI-E)	1.0	07'10/19	52	Power Bottom & USB Board	1.0	07'10/19
18	VGA(STRAP)	1.0	07'10/19	53	Power Design Diagram	1.0	07'10/19
19	VGA(GDDR)	1.0	07'10/19	54	DCIN&Charger	1.0	07'10/19
20	VGA(MULTIUSE)	1.0	07'10/19	55	SYS Power (+3_3V/+5V)	1.0	07'10/19
21	VGA(LVDS/VDAC )	1.0	07'10/19	56	SYS Power(+1_5V/+1_05V)	1.0	07'10/19
22	VRAM(GDDR)	1.0	07'10/19	57	DDR2 Power(+1_8V/+0_9V)	1.0	07'10/19
23	VGA(POWER) 1/3	1.0	07'10/19	58	CPU Power_VHCORE	1.0	07'10/19
24	VGA(POWER) 2/3	1.0	07'10/19	59	VGA Power(+1_2V/+1_2V)	1.0	07'10/19
25	VGA(POWER) 3/3	1.0	07'10/19	60	Others power plane	1.0	07'10/19
26	VRAM(BYPASS)	1.0	07'10/19	61	OVP protection	1.0	07'10/19
27	CRT	1.0	07'10/19	62	HOLE	1.0	07'10/19
28	LVDS	1.0	07'10/19	63	History ( 1 )	1.0	07'10/19
29	ICH8-M( PCI/USB ) 1/5	1.0	07'10/19	64	History ( 2 )	1.0	07'10/19
30	ICH8-M( LPC,IDE,SATA )2/5	1.0	07'10/19	65	History ( 3 )	1.0	07'10/19
31	ICH8-M( GPIO) 3/5	1.0	07'10/19	66	History ( 4 )	1.0	07'10/19
32	ICH8-M( POWER) 4/5	1.0	07'10/19	67	History ( 5 )	1.0	07'10/19
33	ICH8-M( GND) 5/5	1.0	07'10/19	68			
34	SATA HDD/CD-ROM	1.0	07'10/19	69			
35	EC+KBC(3910)	1.0	07'10/19	70			

M730 Main Board

M/B P/N: 1P-0079100-8010 (FUBAI)  
1P-0079500-8010 (HANSTAR)  
1P-0079G00-8010 (TRIPOD)

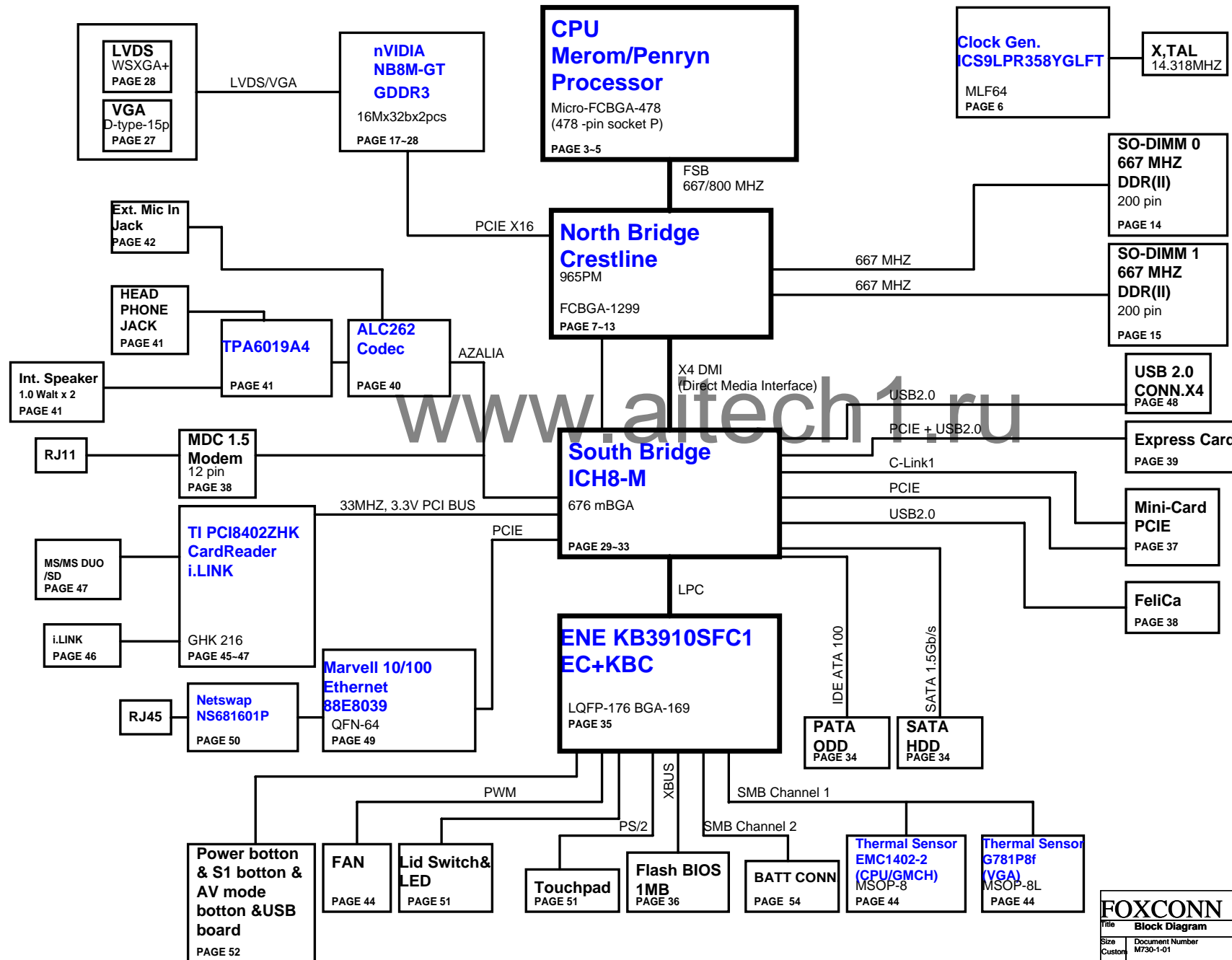
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1P-1079500-8010 (HANSTAR)  
1P-1079G00-8010 (TRIPOD)

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1P-1079501-8010 (HANSTAR)  
1P-1079G01-8010 (TRIPOD)

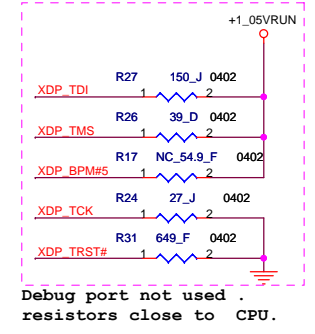
P. Leader	Check by	Design by

<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title Index Page		
Size A3	Document Number M730-1-01	Rev 1.0
Date: Saturday, October 13, 2007	Sheet 1	of 67

# M730 (Crestline PM+Gfx Block Diagram)



Layout note:  
no stub on H\_STPCLK TP.  
H\_STPCLK# to be routed in daisy chain fashion from ICH to LPC slot and then to CPU.

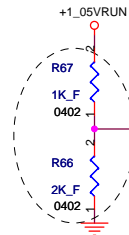


PM\_THRMTRIP#  
should connect to  
ICH8-M and GMCH  
without T-ing (No stub)

ICH8M's GPIO12: VIL---> -0.5V ~ 0.8V  
VIH---> 2.0V ~ 3.3+0.5V  
MEROM's PROCHOT#: VIL---> -0.1V ~ 0.3\*VCCP  
VIH---> 0.7\*VCCP ~ VCCP+0.1

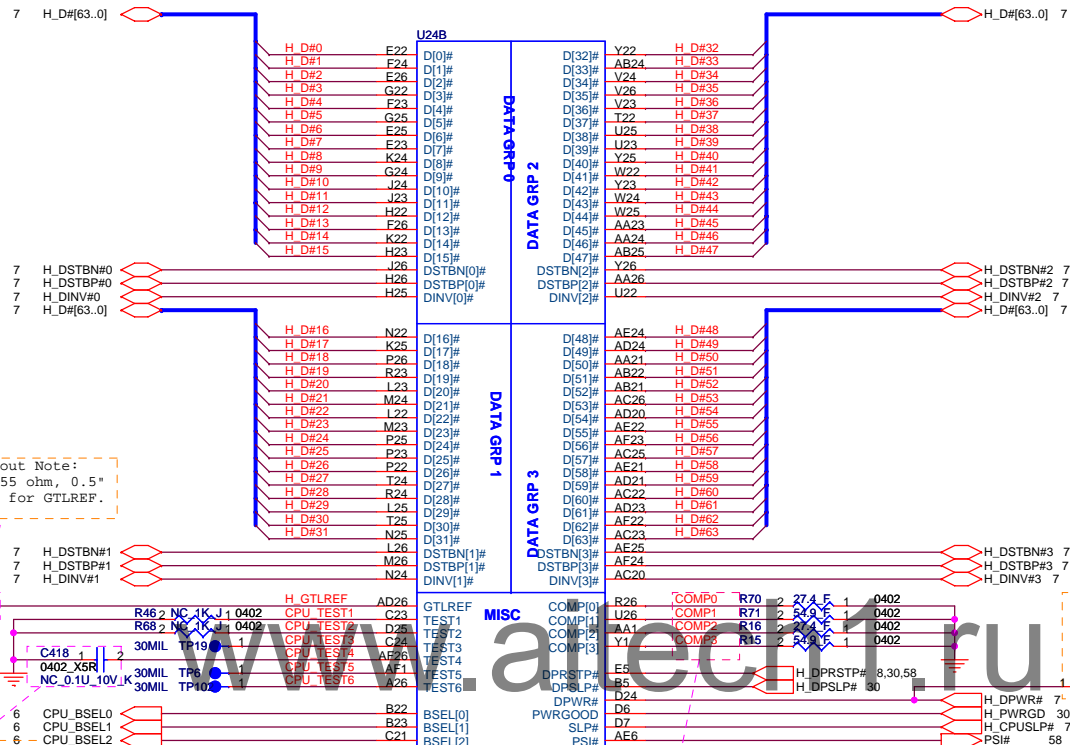
When use U3, R429 and C453  
need change to NC.

Place close to CPU



Place C418 close to the CPU\_TEST4 pin.  
Make sure CPU\_TEST4 routing is reference  
to GND and away from other noisy signals.

Layout Note:  
Zo=55 ohm, 0.5"  
max for GTLREF.



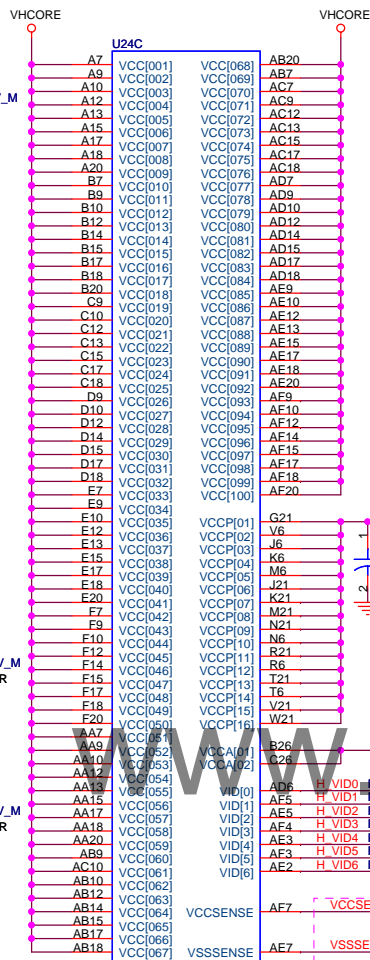
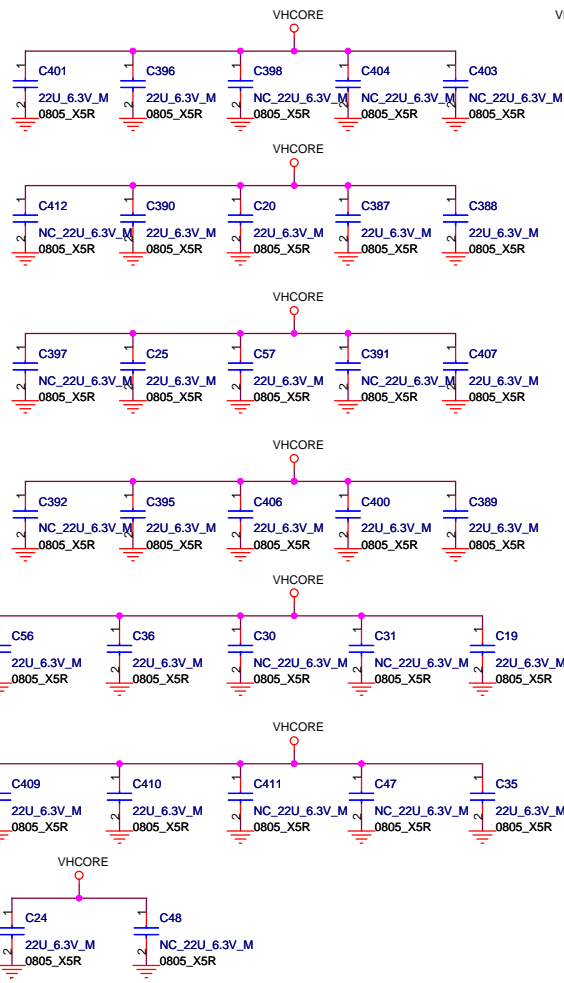
CPU SOCKET\_478P  
FOX\_P24782A-274M-01

Layout Note:  
Comp0,2 connect with Zo=27.4 ohm, make  
trace length shorter then 0.5".  
Comp1,3 connect with Zo=55 ohm, make  
trace length shorter then 0.5".

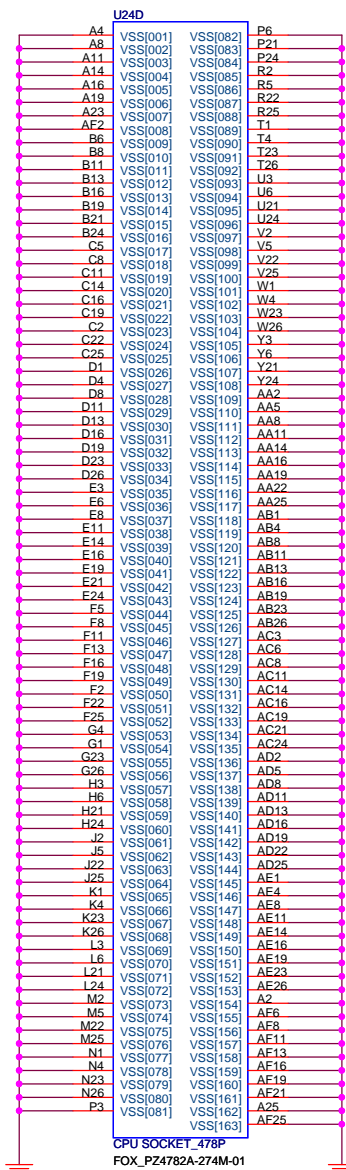
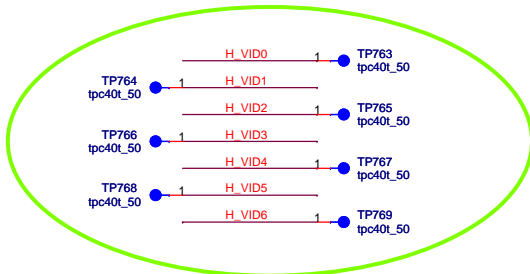
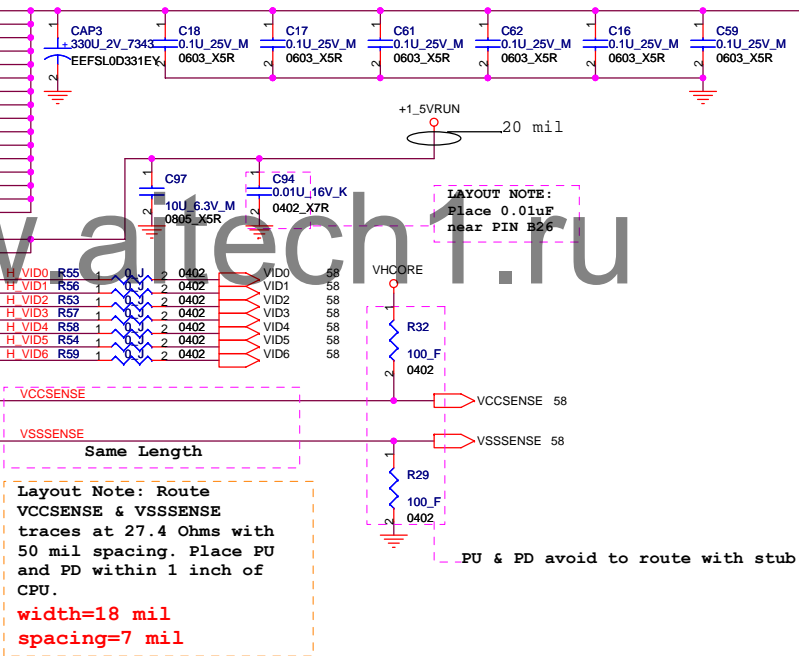
Layout:  
Connect test  
point with no  
stub

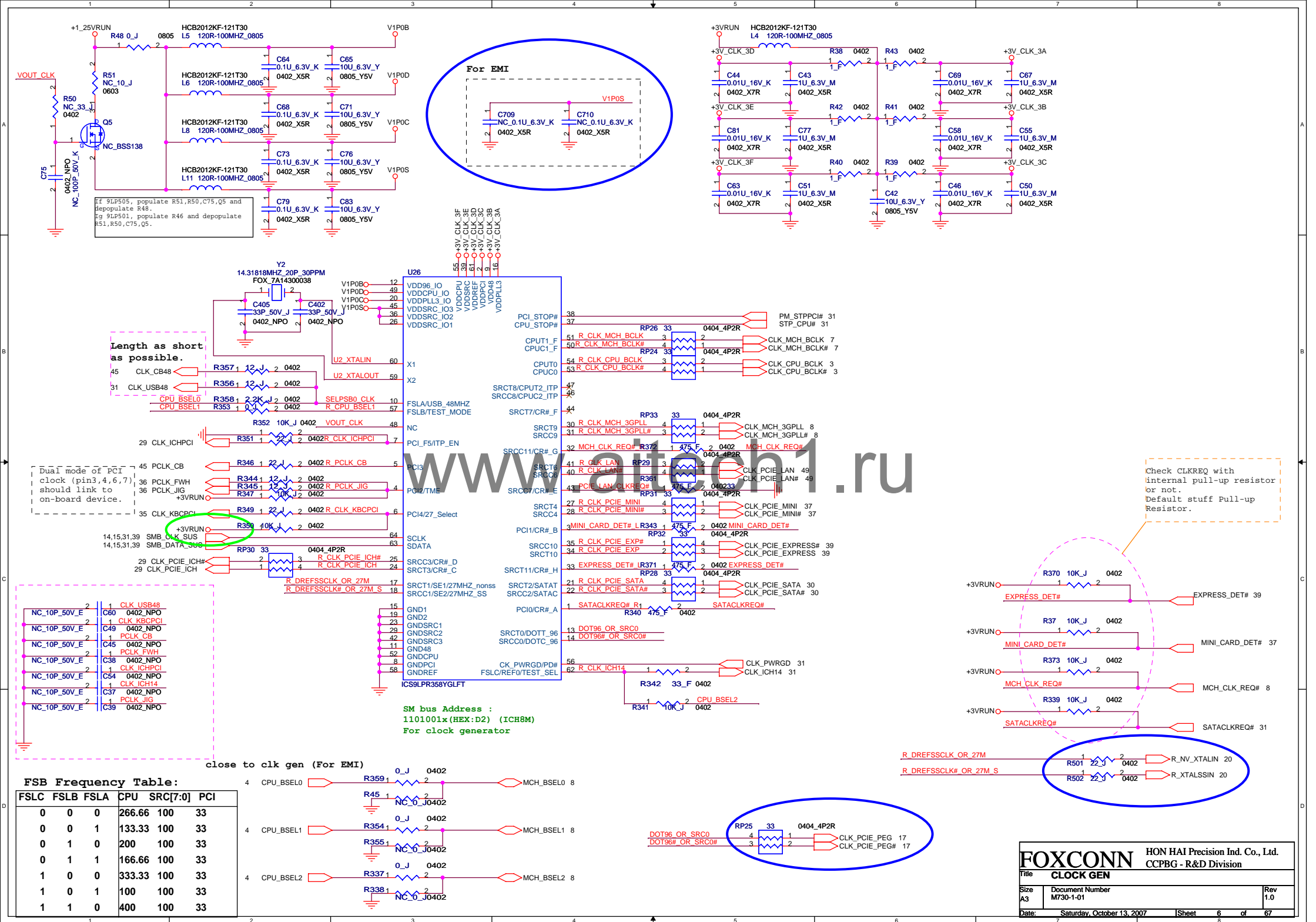
IMVP6 (ISL6262ACRZ-T)  
cpu PSI# <-> ISL6262ACRZ-T PSI#  
ISL6262ACRZ-T: VIHmin=0.315V  
VILmax=0.735V  
(ref. IMVP-6 NO:18904)

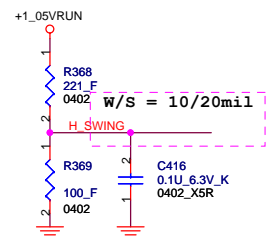




CPU\_VCCA----->120mA  
CPU\_VCCP----->2.5A  
CPU\_VCC----->36A







W/S = 10/20mil  
H\_RCOMP



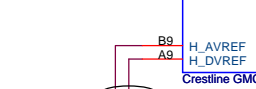
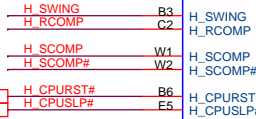
H\_SCOMP



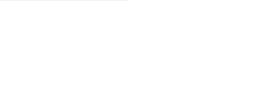
H\_SCOMP#



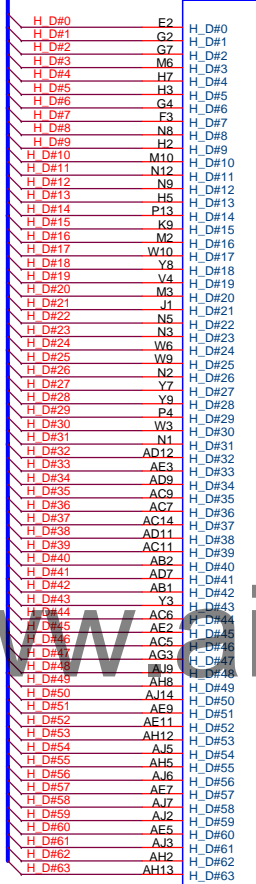
Place Cap.  
near GMCH  
within 100  
mils.



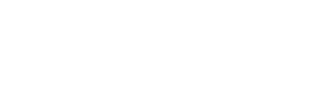
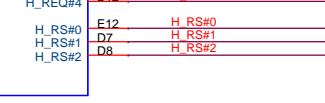
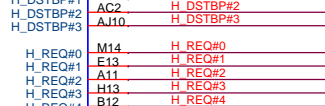
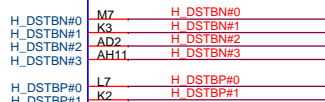
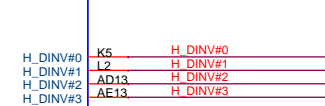
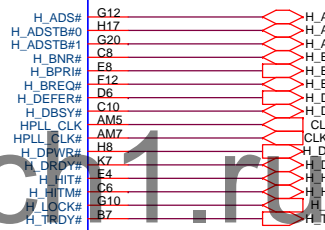
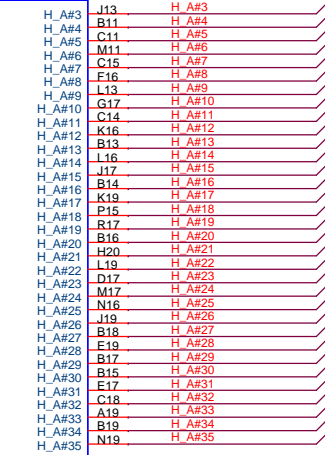
20 mil

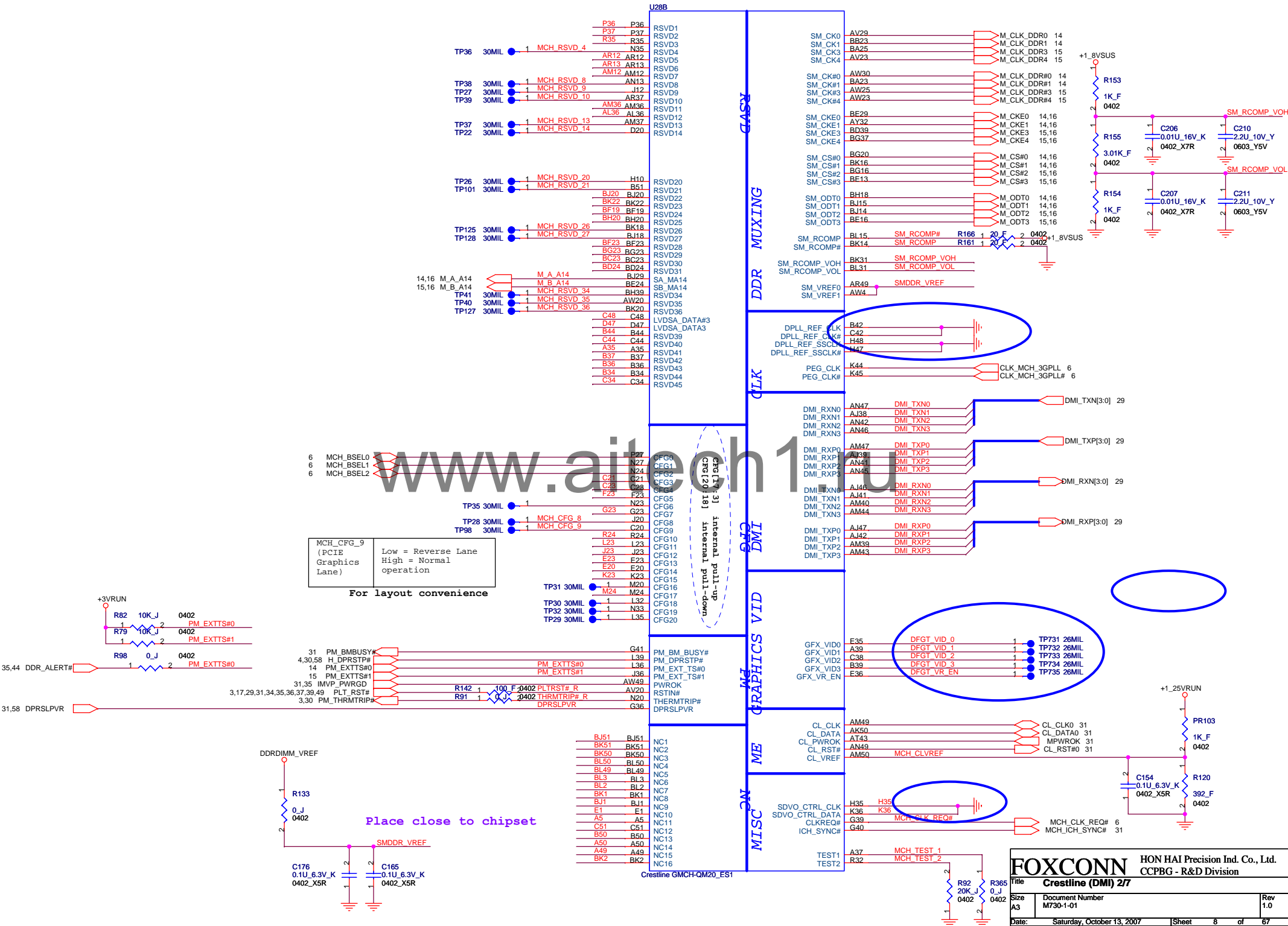


U28A



HOST





MCH\_CFG\_9 (PCIe Graphics Lane)  
Low = Reverse Lane  
High = Normal operation

For layout convenience

Place close to chipset

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CCPBG - R&D Division

Title

Crestline (DMI) 2/7

Size

A3

Document Number

M730-1-01

Rev

1.0

Date:

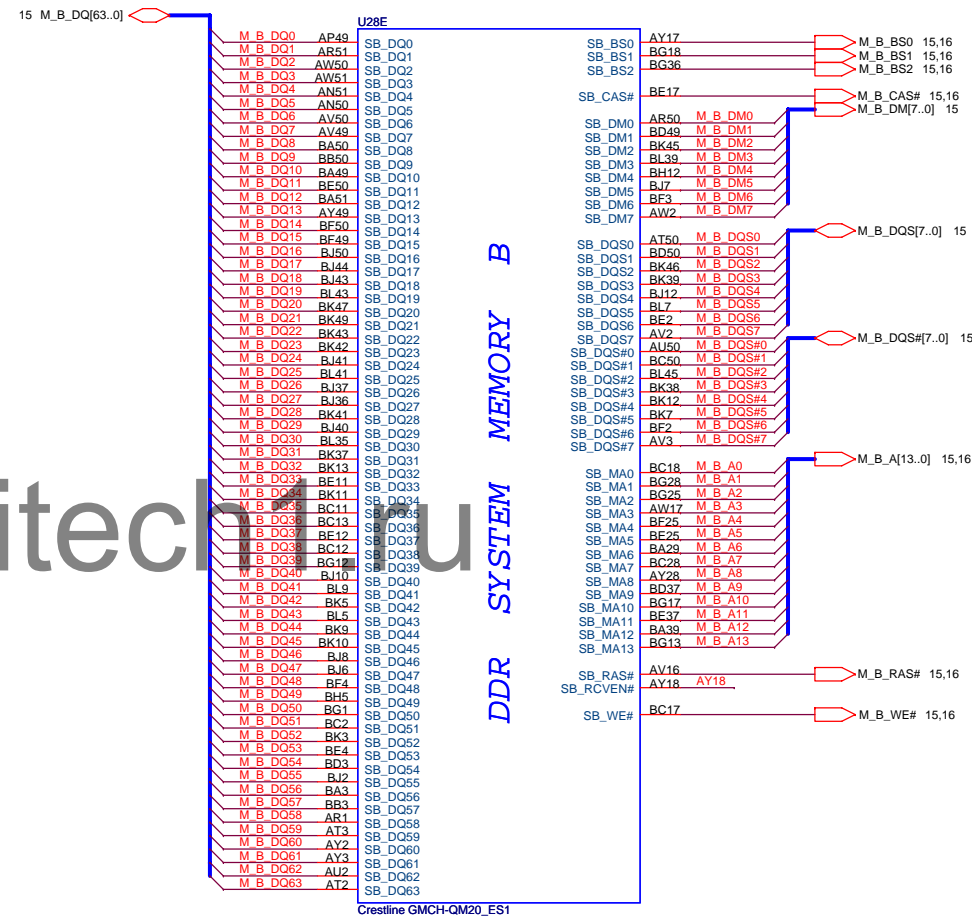
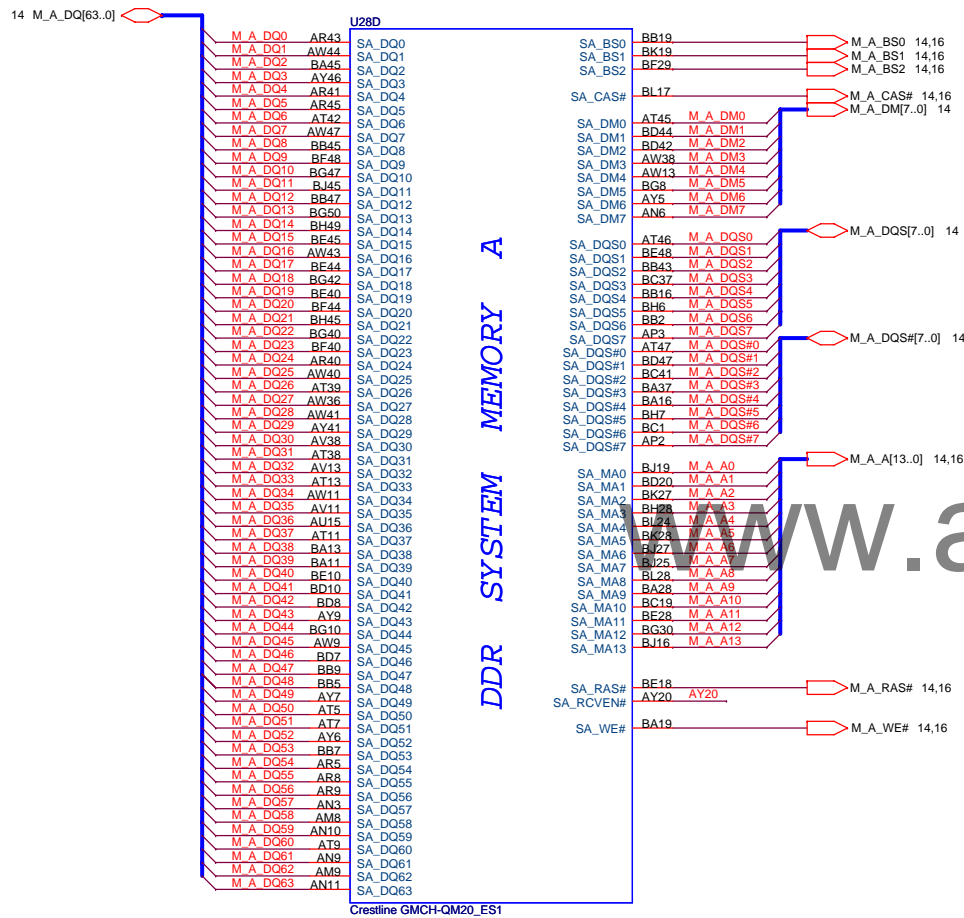
Saturday, October 13, 2007

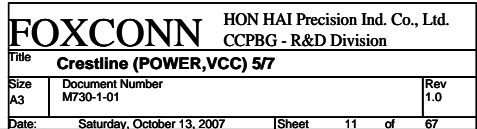
Sheet

8 of 67



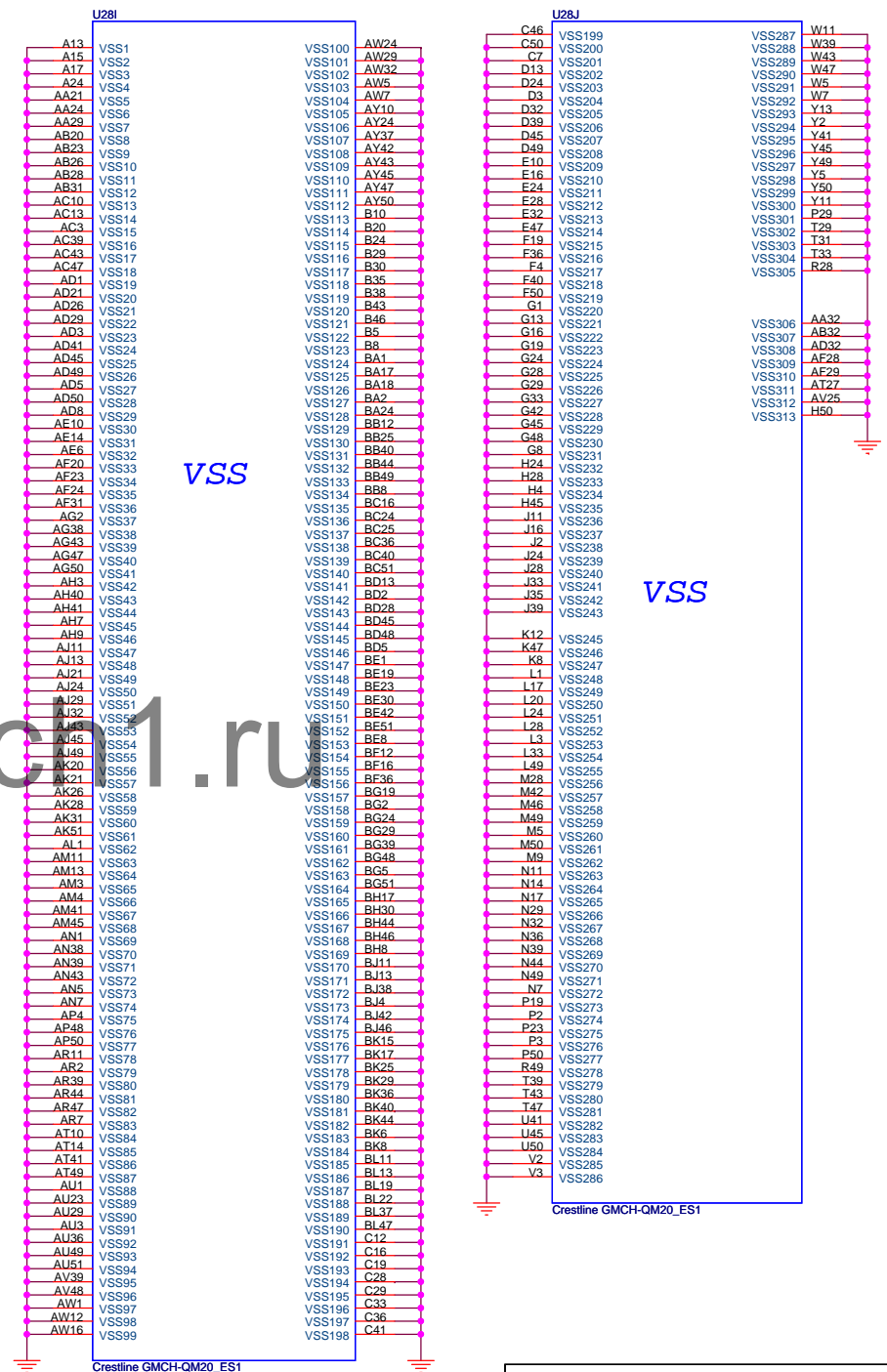




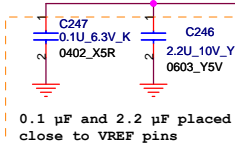




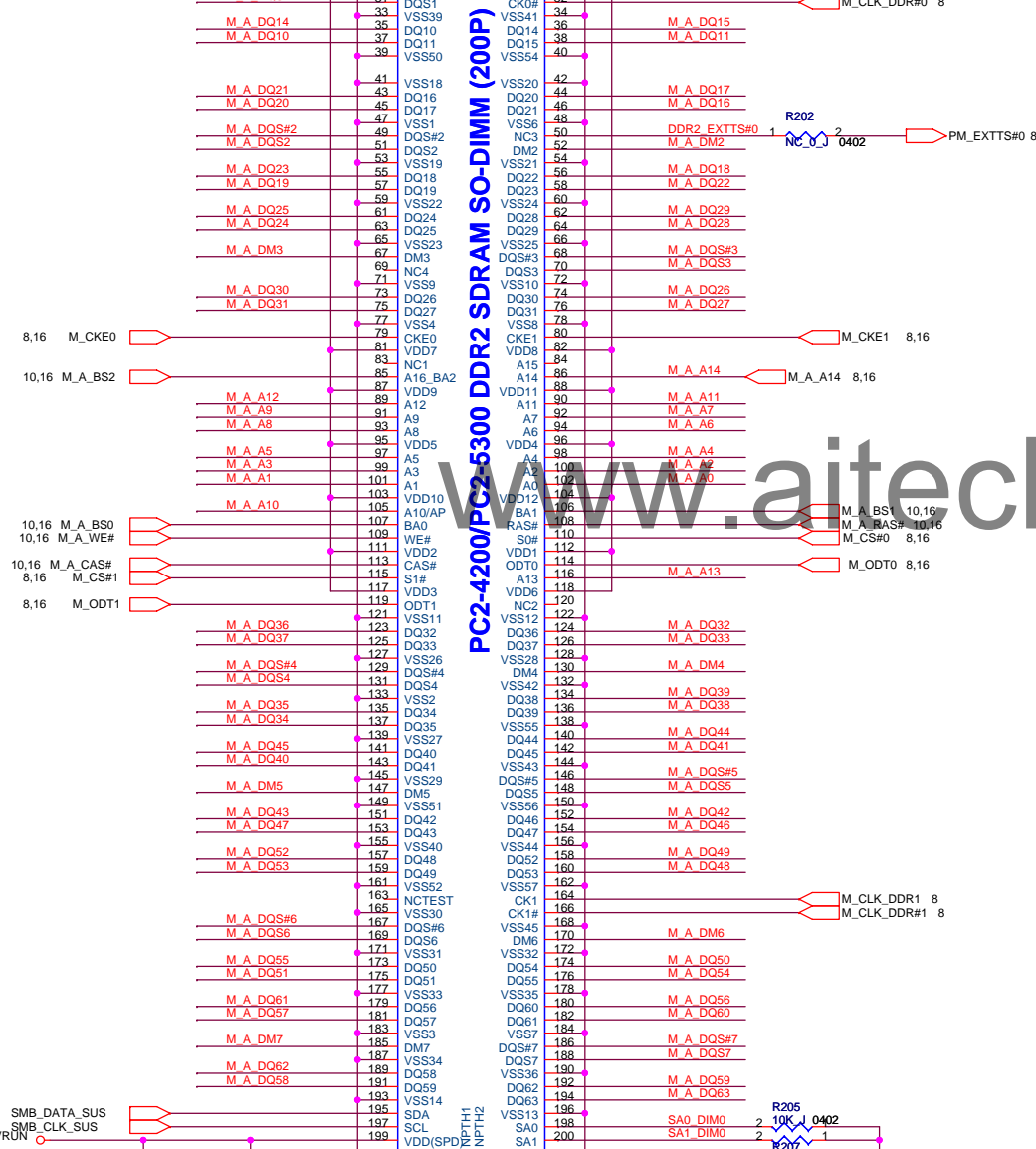




1.8V per DIMM=3.08A



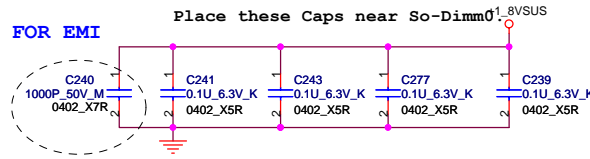
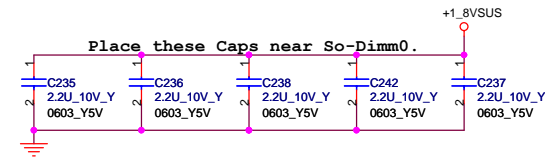
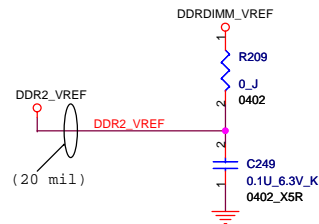
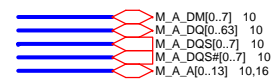
"Intel check list suggest a 330uF"

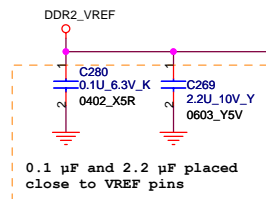


DIMM\_0

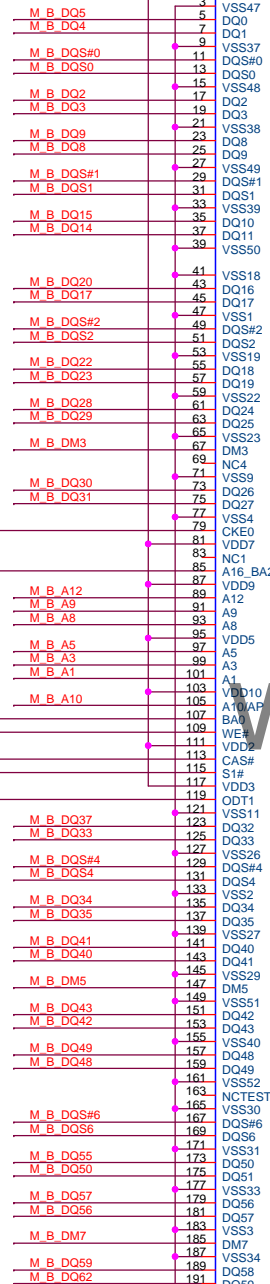
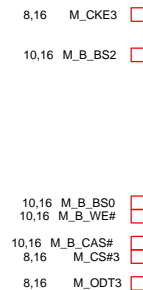
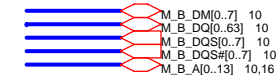
SMBus Address: A0 (W) / A1 (R)

Place DIMM\_0 near GMCH

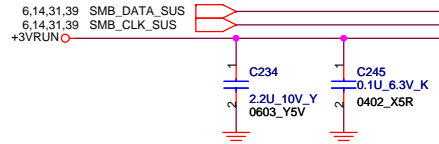
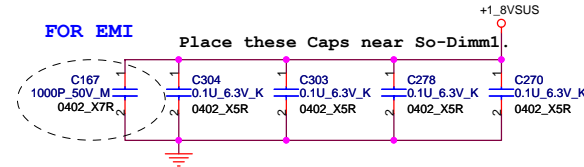
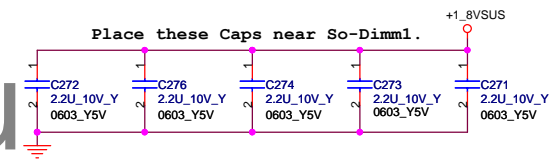
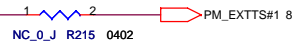




1.8V per DIMM=3.08A



PC2-4200/PC2-5300 DDR2 SDRAM SO-DIMM (200P)



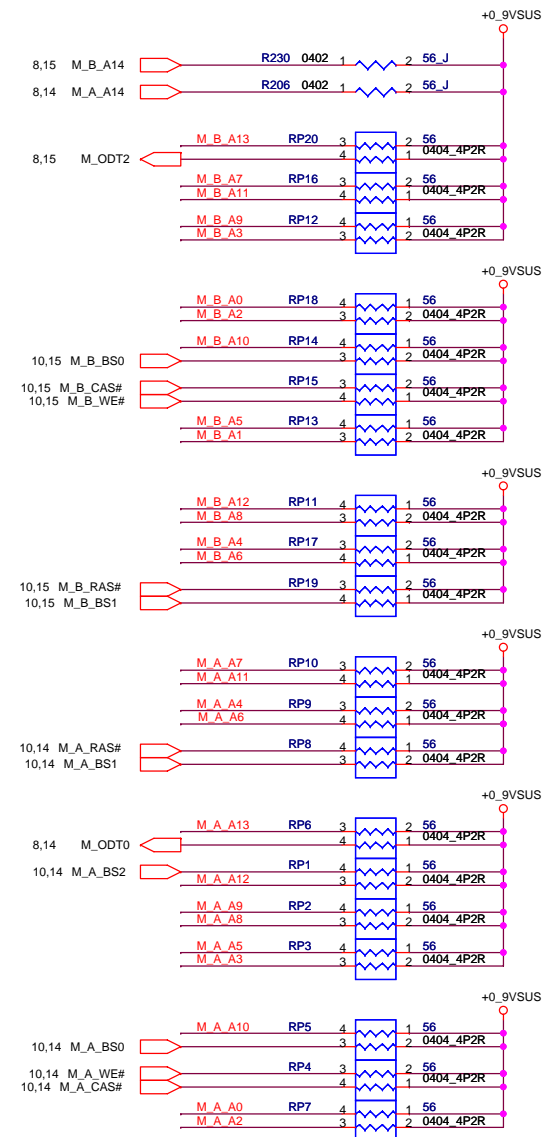
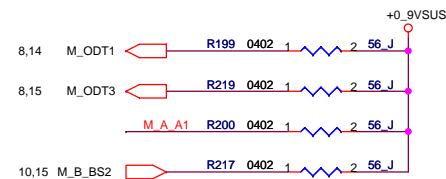
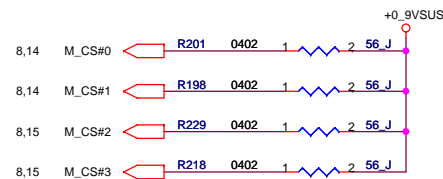
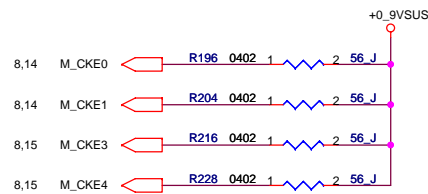
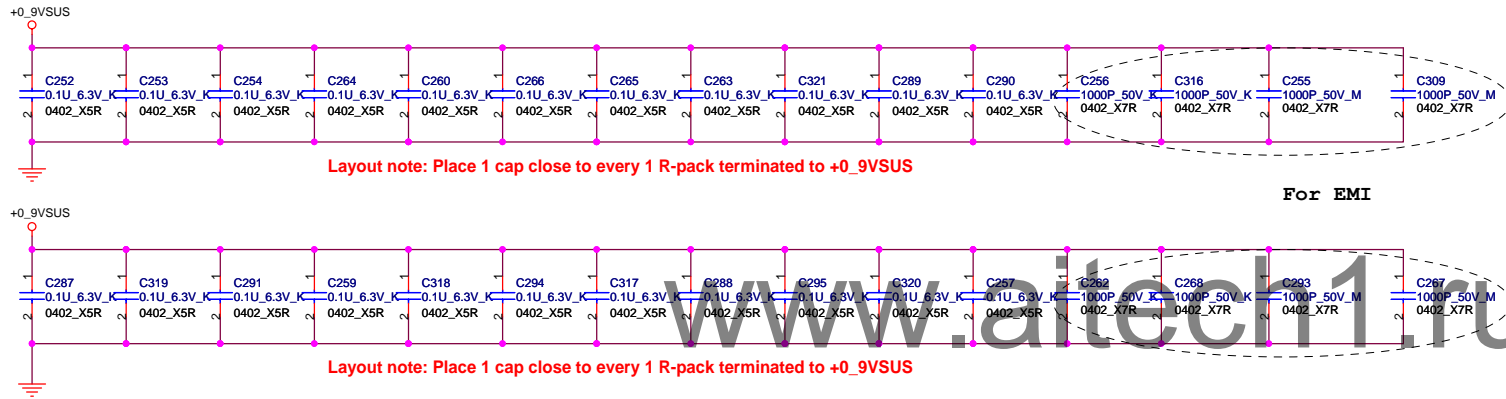
DIMM\_1

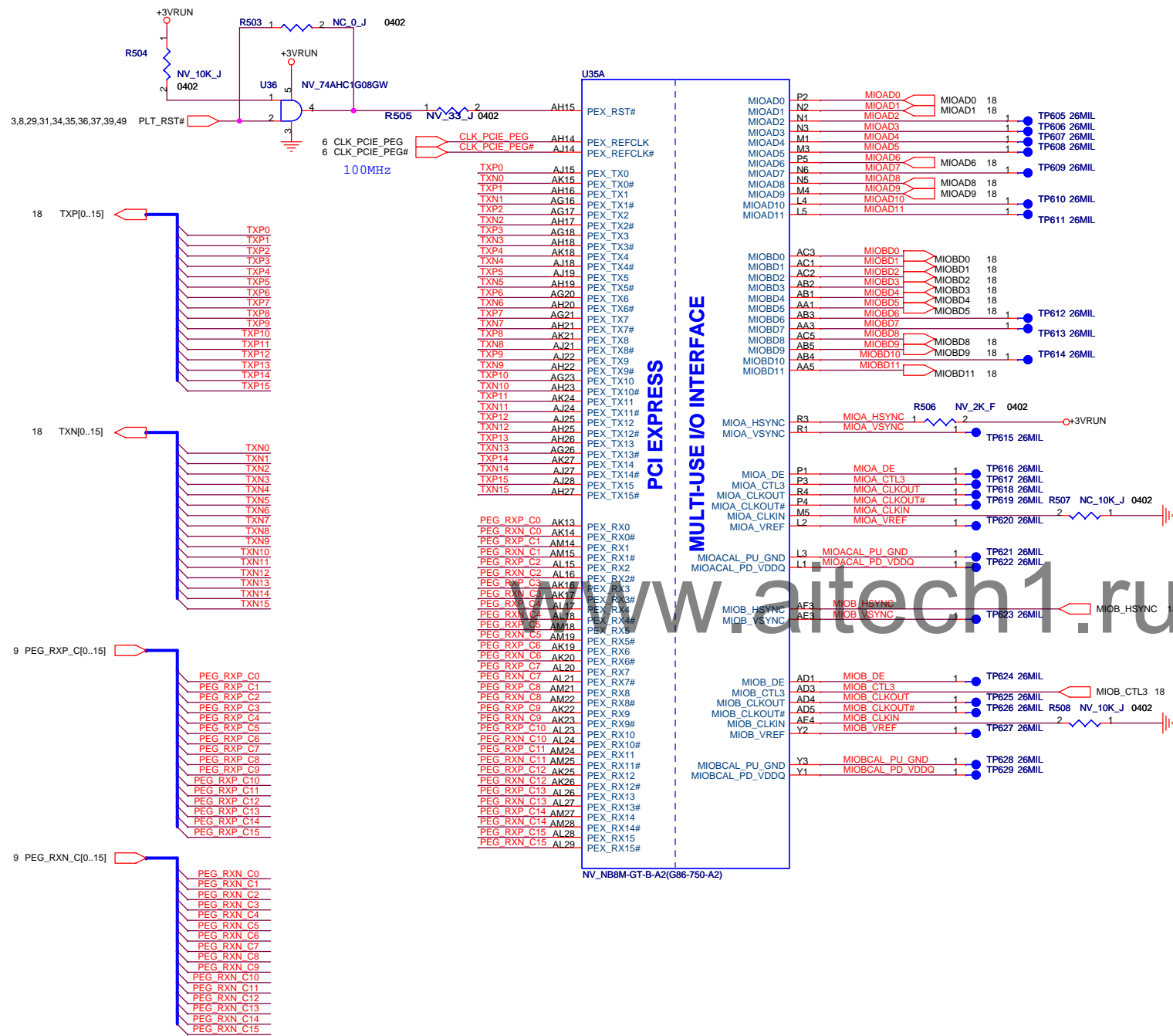
SMBus Address: A4 (W) / A5 (R)

DIMM\_1 is placed farther from the GMCH than DIMM\_0



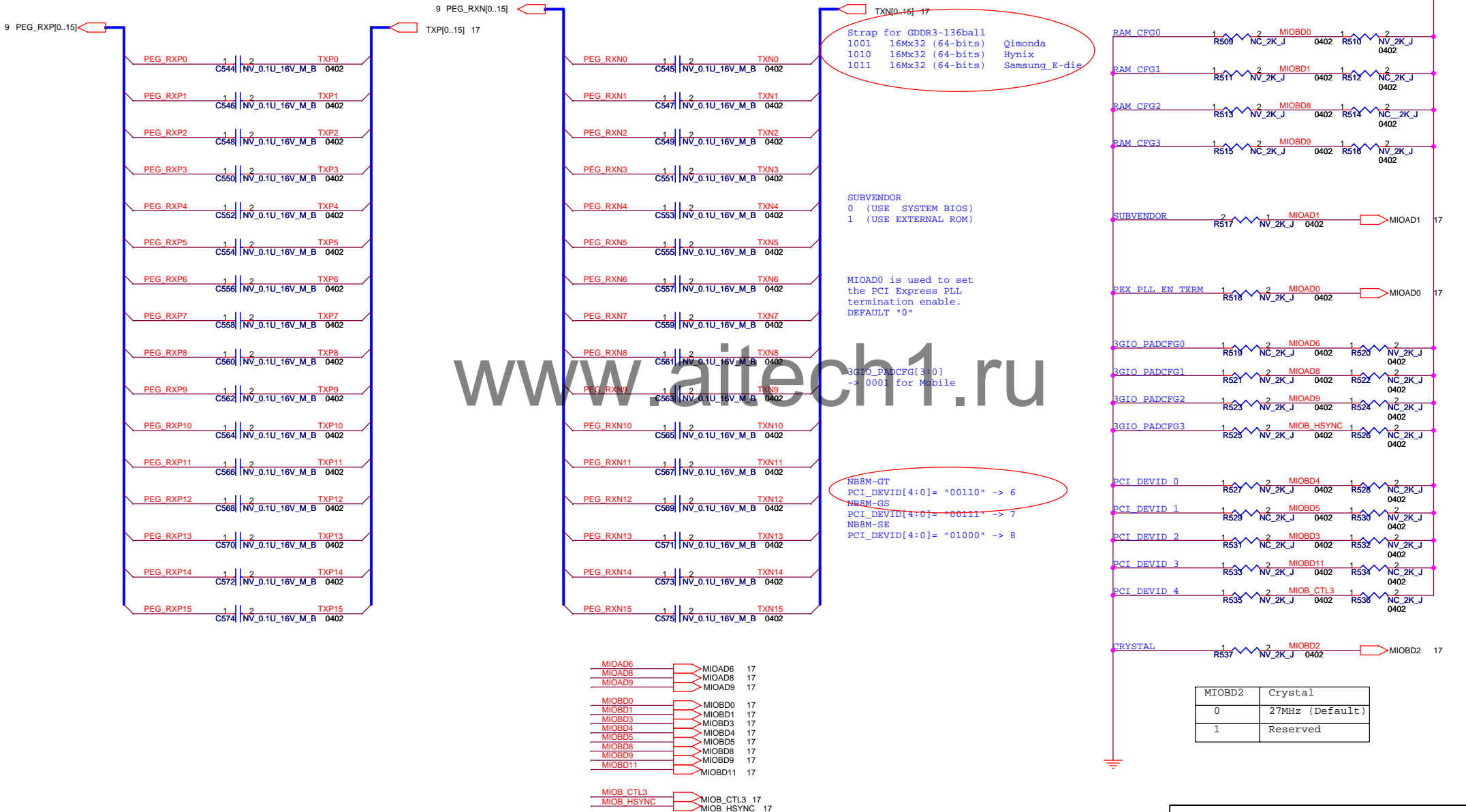
FOXCONN			HON HAI Precision Ind. Co., Ltd.	
Title			CCPBG - R&D Division	
M730-1-01			Rev 1.0	
Date: Saturday, October 13, 2007			Sheet 15 of 67	

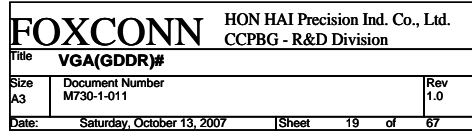




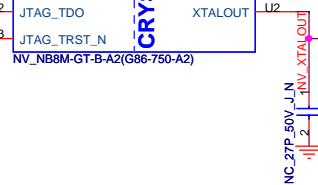
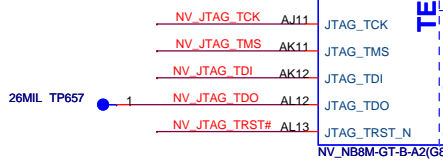
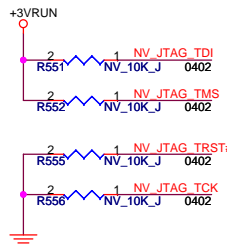
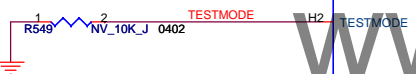
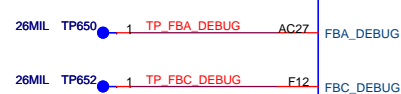
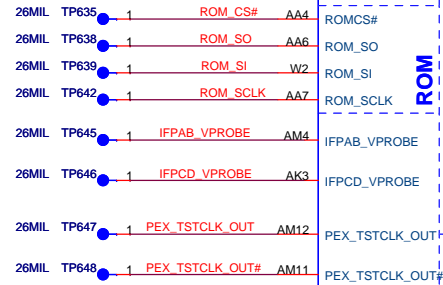
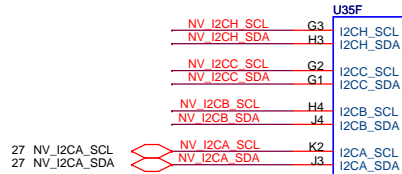
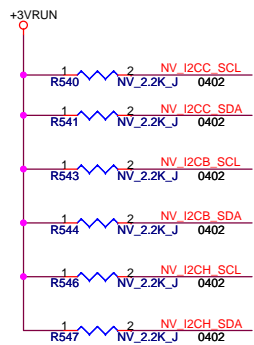
SKU			
Vender	Qimonda (Infineon)	HYNIX	Samsung
Vendor PN	HYB18H512321BF-14	HY5RS123235BFP-14	K4J52324QE-BC14
H.H PN	13-HYB18H5-3003	13-HY5RS12-3001	13-K4J5232-3001
Configuration	NB8M-GT with 2pcs (16Mx32) GDDR3		
LOCATION	Stuff R511,R510	Stuff R512,R509	Stuff R512,R510
	No Stuff R512,R509	No Stuff R511,R510	No Stuff R511,R509

FAE: TV Mode Strap no use, remove.  
(MIOAD7, MIOAD10, MIOBD6)









**GENERAL SIGNALS**

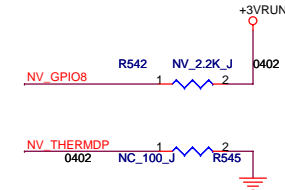
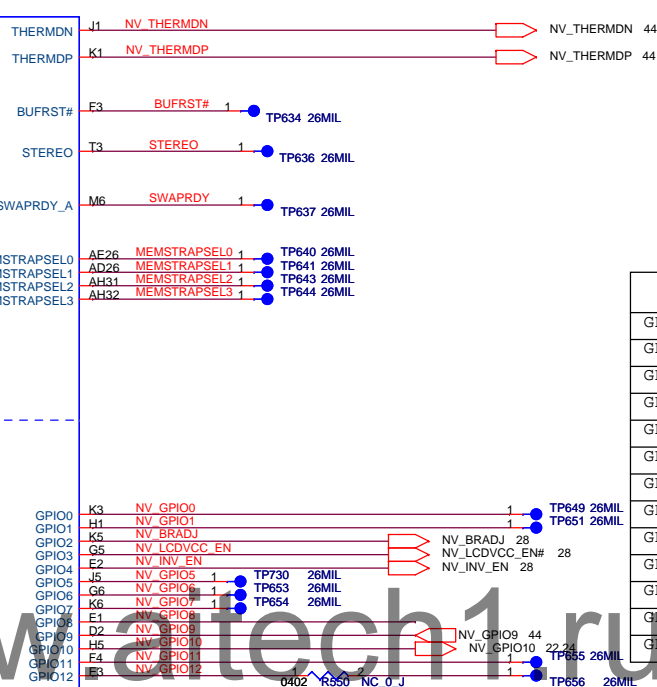
**I2C**

**ROM**

**TEST SIGNAL**

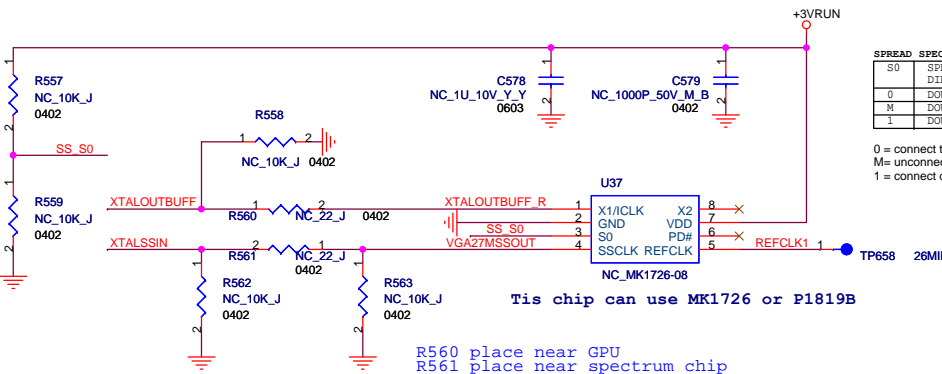
**GPIO**

**CRYSTAL**



	I/O	Internal pull low	GPIO TABLE
GPIO0	I	Yes	TP
GPIO1	I	Yes	TP
GPIO2	O	Yes	Panel Brightness (PWM) <b>Active High</b>
GPIO3	O	No	Panel Power Enable <b>Active Low</b>
GPIO4	O	Yes	Panel Backlight On/Off <b>Active High</b>
GPIO5	O	Yes	TP
GPIO6	O	Yes	TP
GPIO7	O	Yes	TP
GPIO8	OD	No	
GPIO9	OD	No	THERM <b>Active Low</b>
GPIO10	O	No	Memory Vref switch
GPIO11	O	No	TP
GPIO12	I	--	TP

NB8M: XTALIN use 3.3V level



Tis chip can use MK1726 or P1819B

R560 place near GPU  
R561 place near spectrum chip

S0	SPREAD DIRECTION	Spread Percentage(%)
0	DOWN	-1.8
M	DOWN	-0.6
1	DOWN	-2.5

SRS PIN3	SPREAD DIRECTION	Spread Percentage(%)
0	DOWN	-1.25
1	DOWN	-1.75

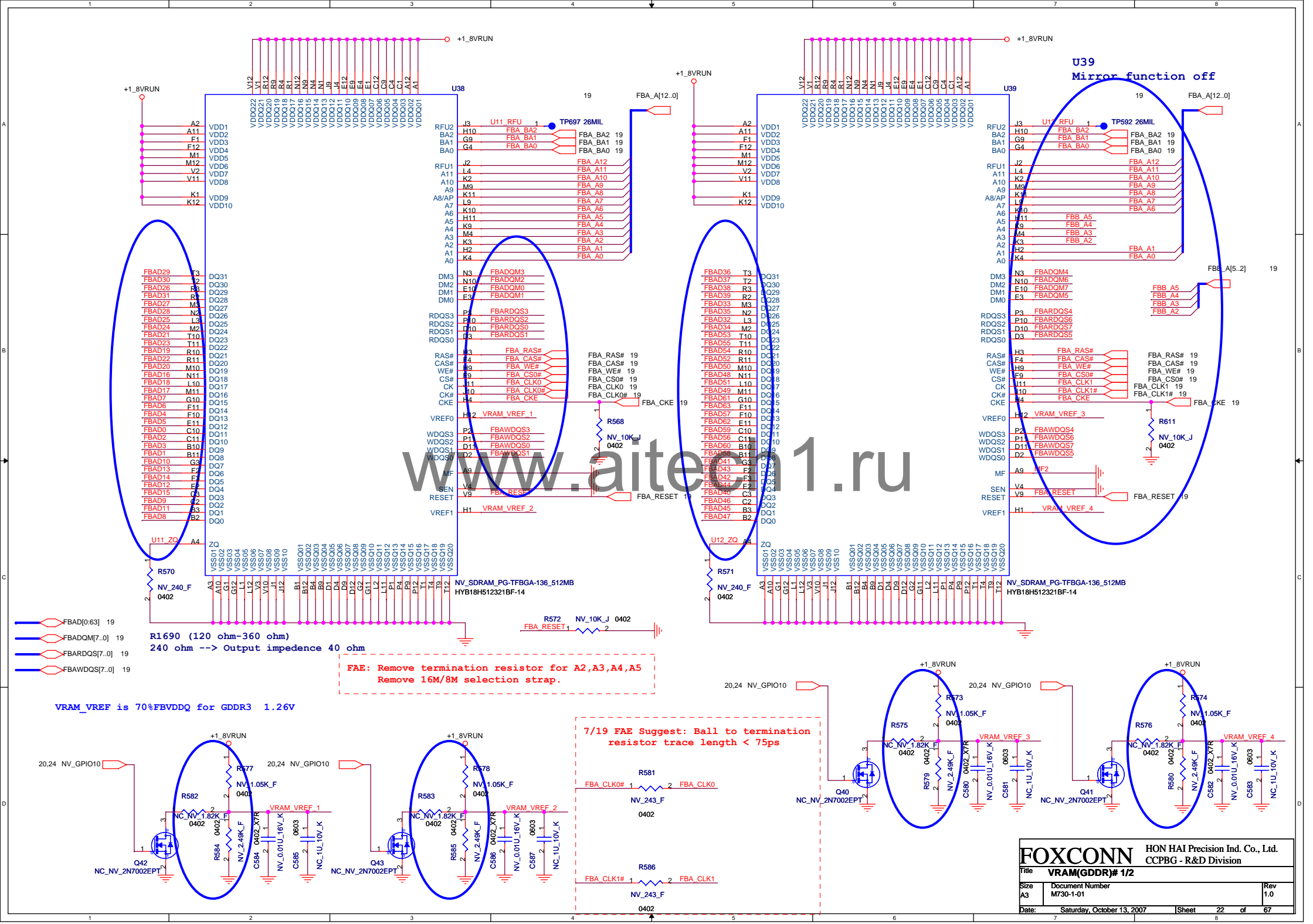
0 = connect to GND  
M = unconnected  
1 = connect directly to VDD

nVidia support Down -1.25%

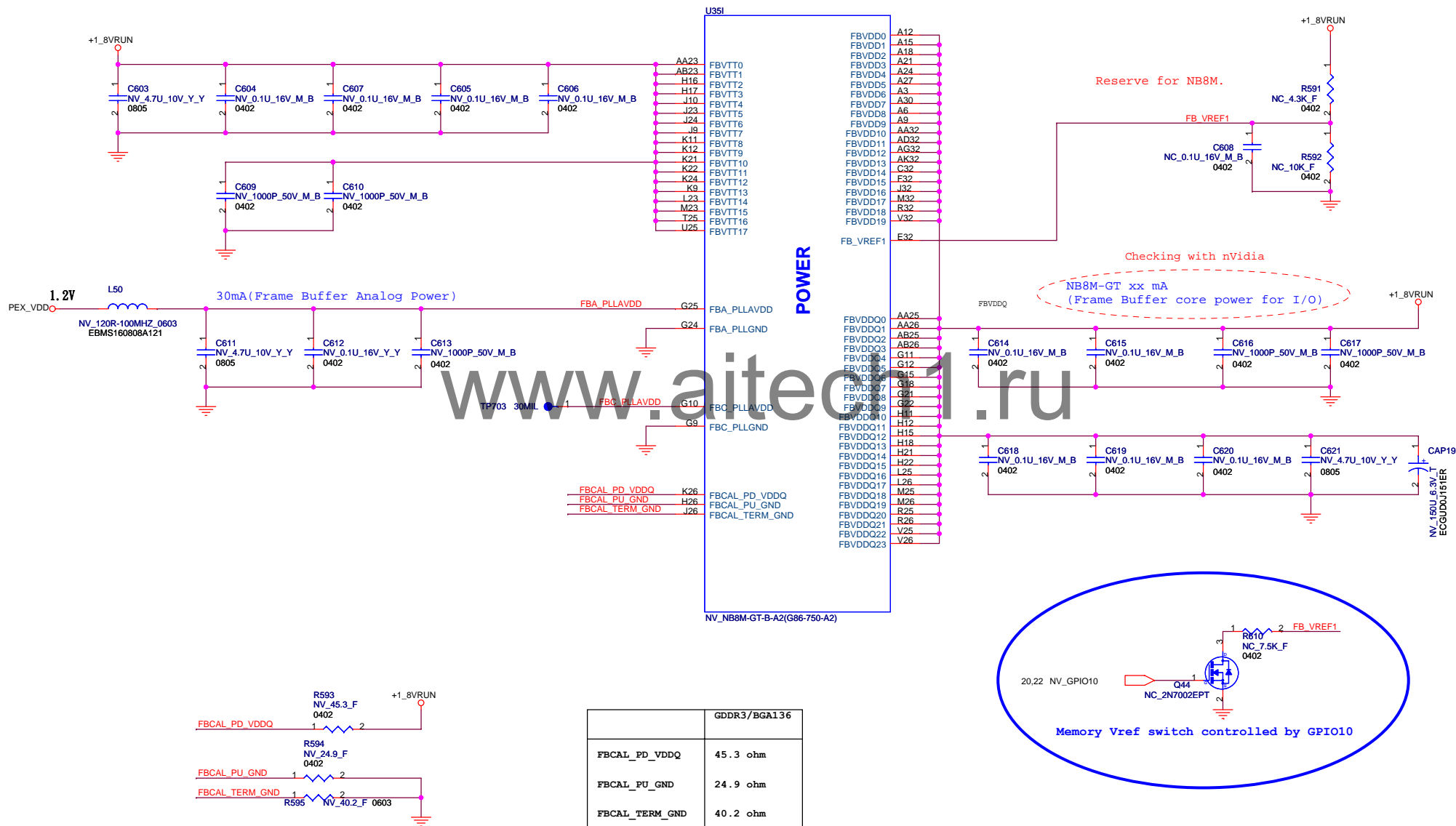
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title <b>VGA(MULTIUSE)</b>		CCPBG - R&D Division	
Size <b>A3</b>	Document Number <b>M730-1-01</b>	Rev <b>1.0</b>	
Date	Saturday, October 13, 2007	Sheet	20 of 67

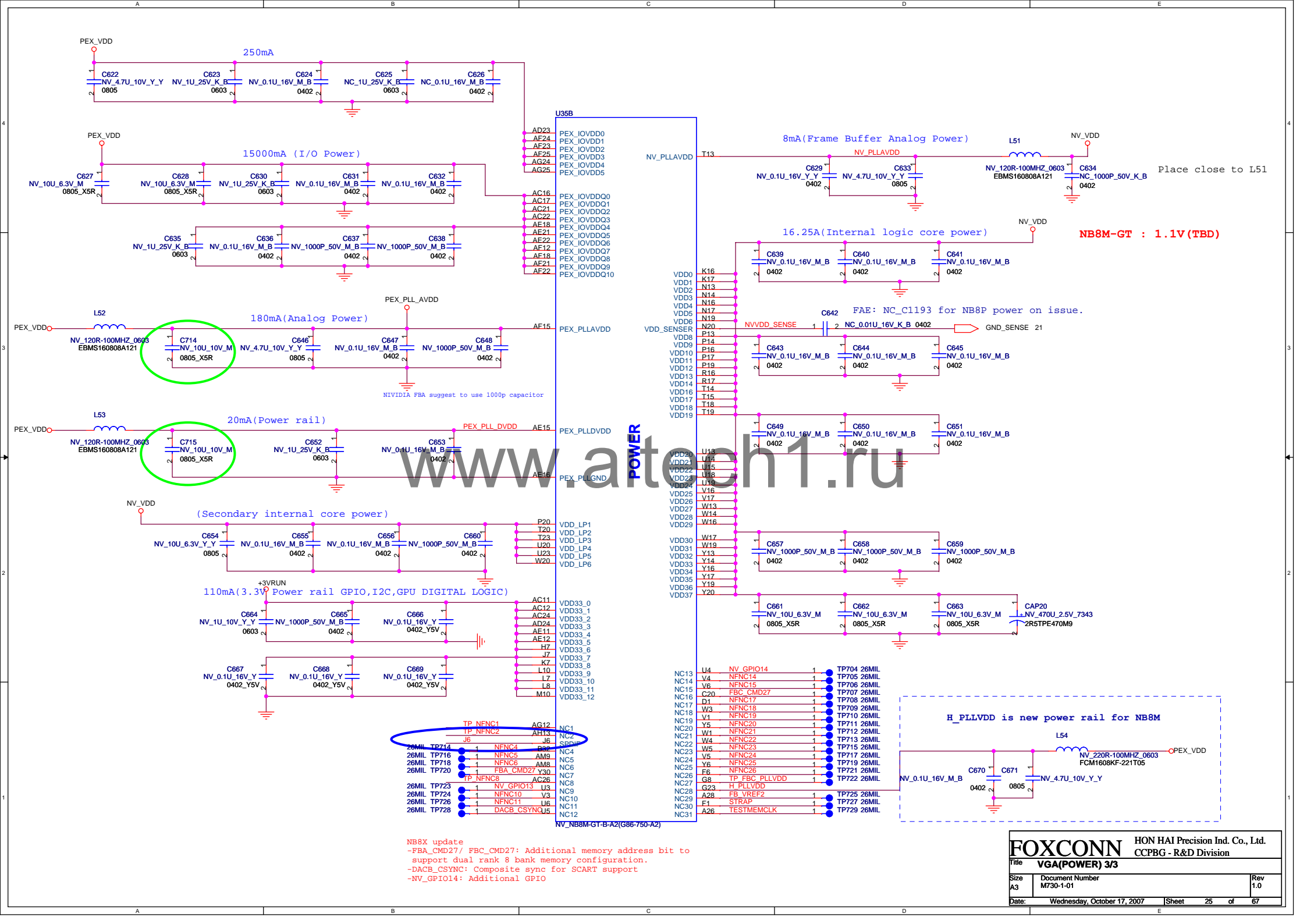






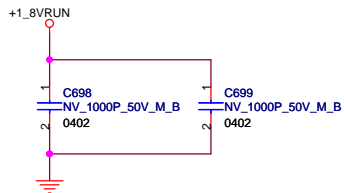
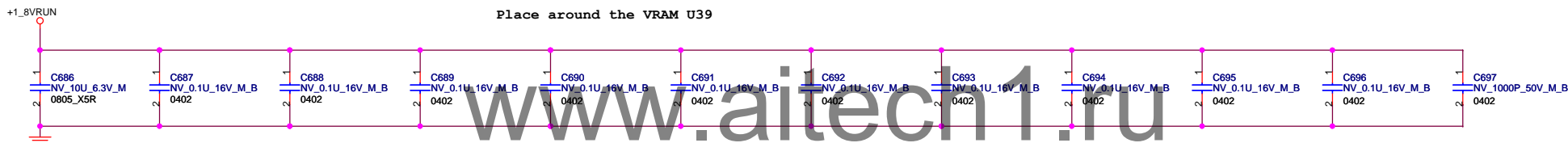
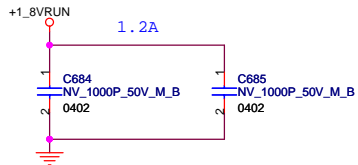
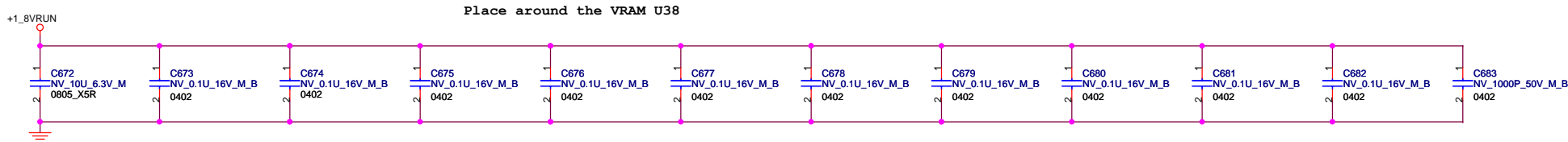


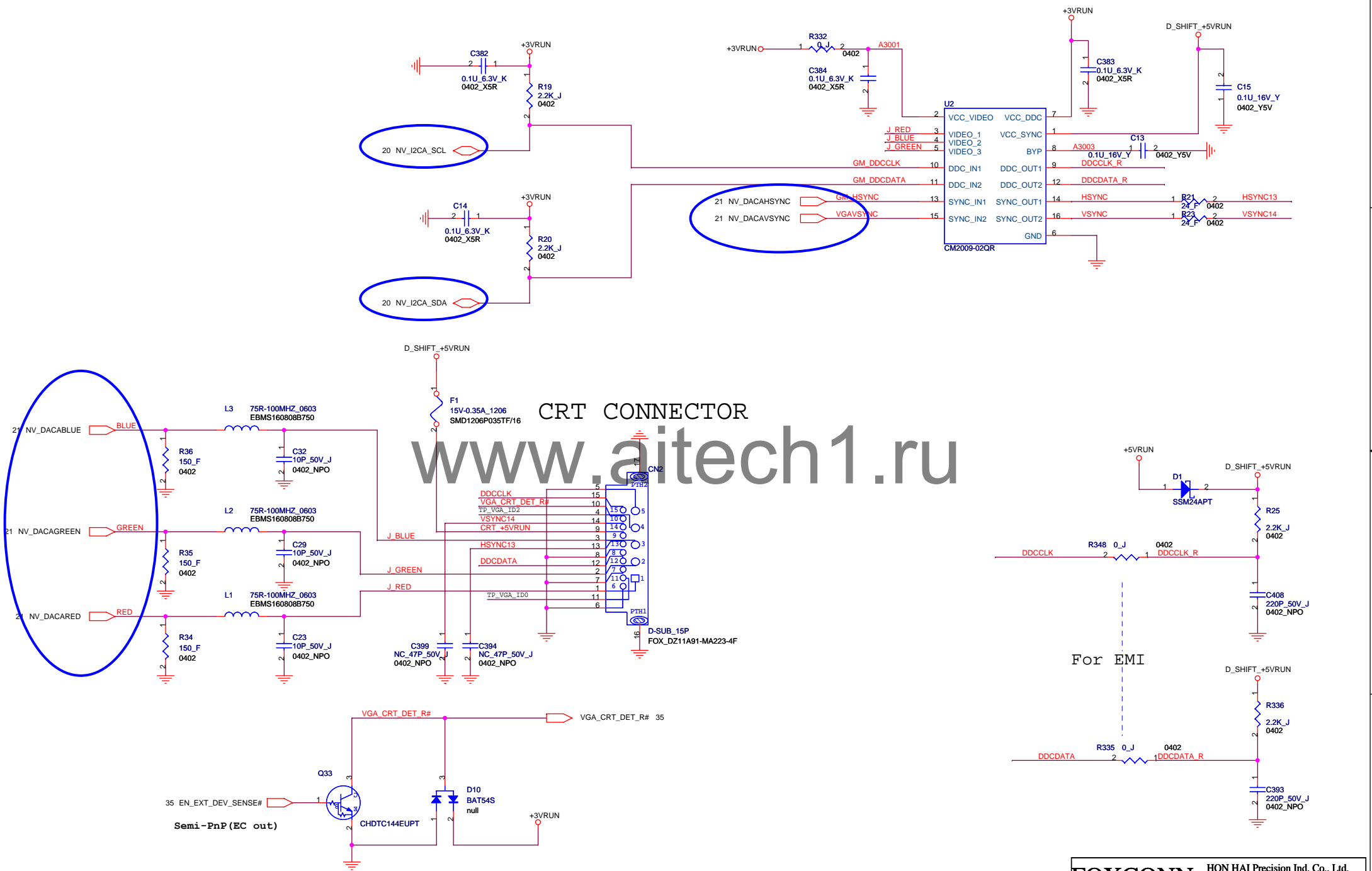




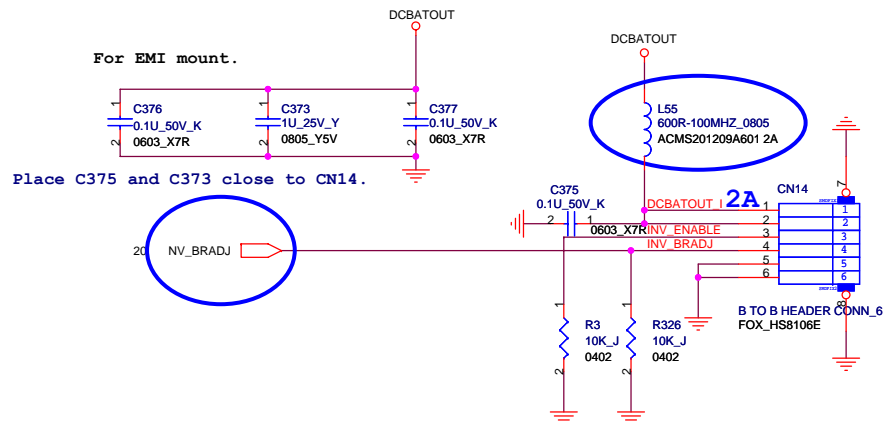
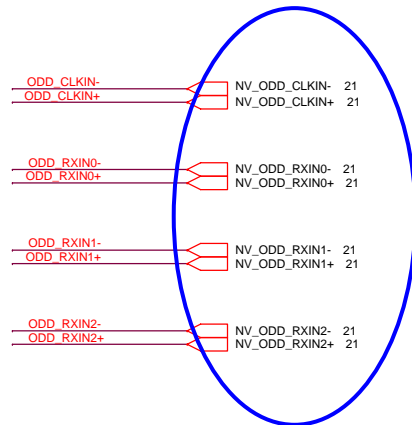
NB8X update

- FBC\_CMD27: Additional memory address bit to support dual rank 8 bank memory configuration.
- DACB\_CSYNQ: Composite sync for SCART support
- NV\_GPIO14: Additional GPIO

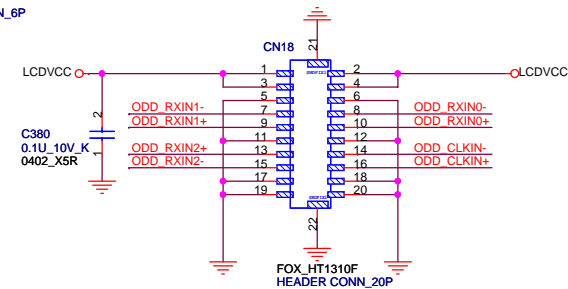




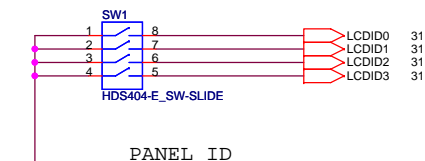
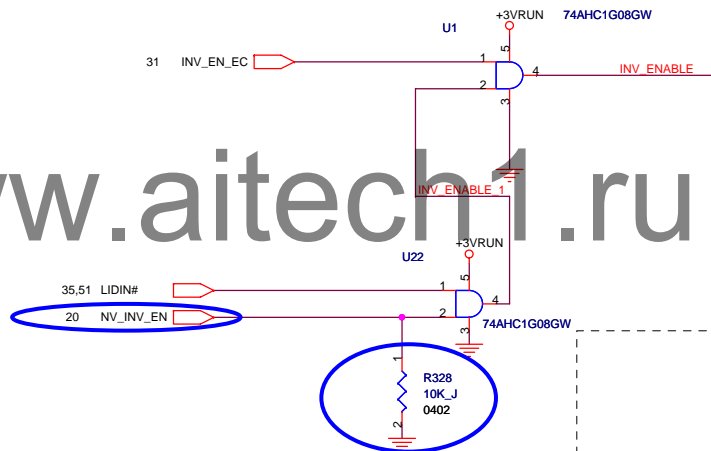
# LVDS



## INVERTER CONN.

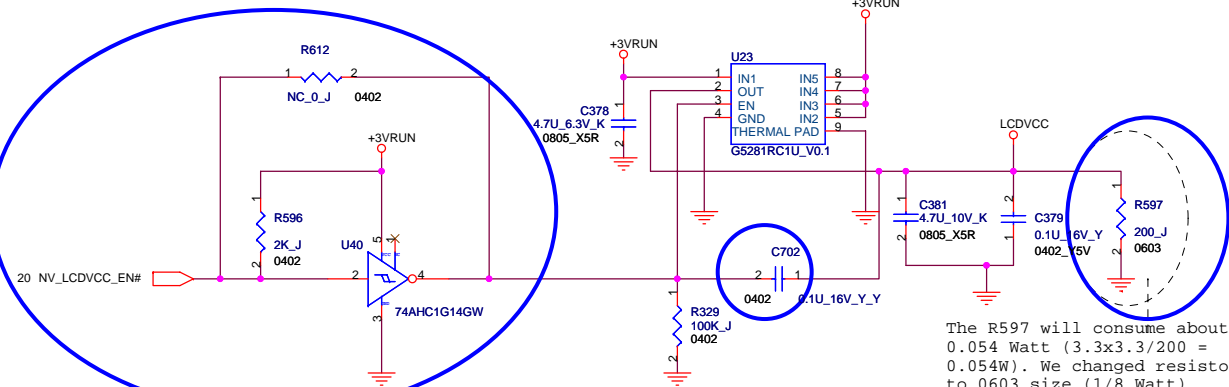


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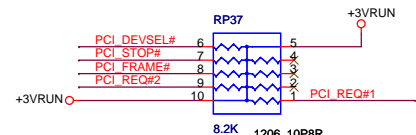
## PANEL ID

Type	WXGA	WXGA	WXGA	WXGA
Size	15.4"W	15.4"W	15.4"W	15.4"W
Vendor	AUO	CPT	LPL	AUO
Device Name	B154EW02V7	CLAA154WB05AN	LP154WX4-TLC5	QD15TL0703
Panel ID Check[3..0]	0001	0010	0011	0100

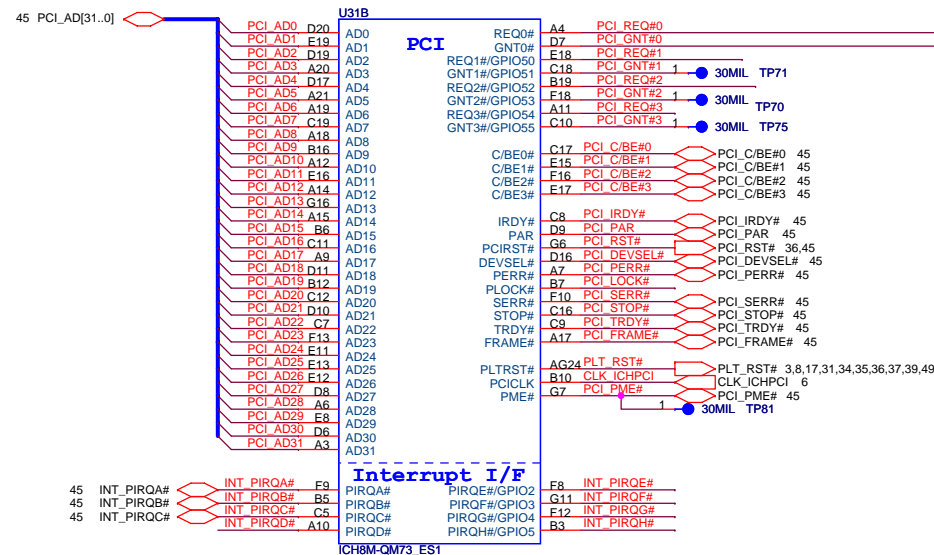


The R597 will consume about 0.054 Watt ( $3.3 \times 3.3 / 200 = 0.054W$ ). We changed resistor to 0603 size (1/8 Watt)

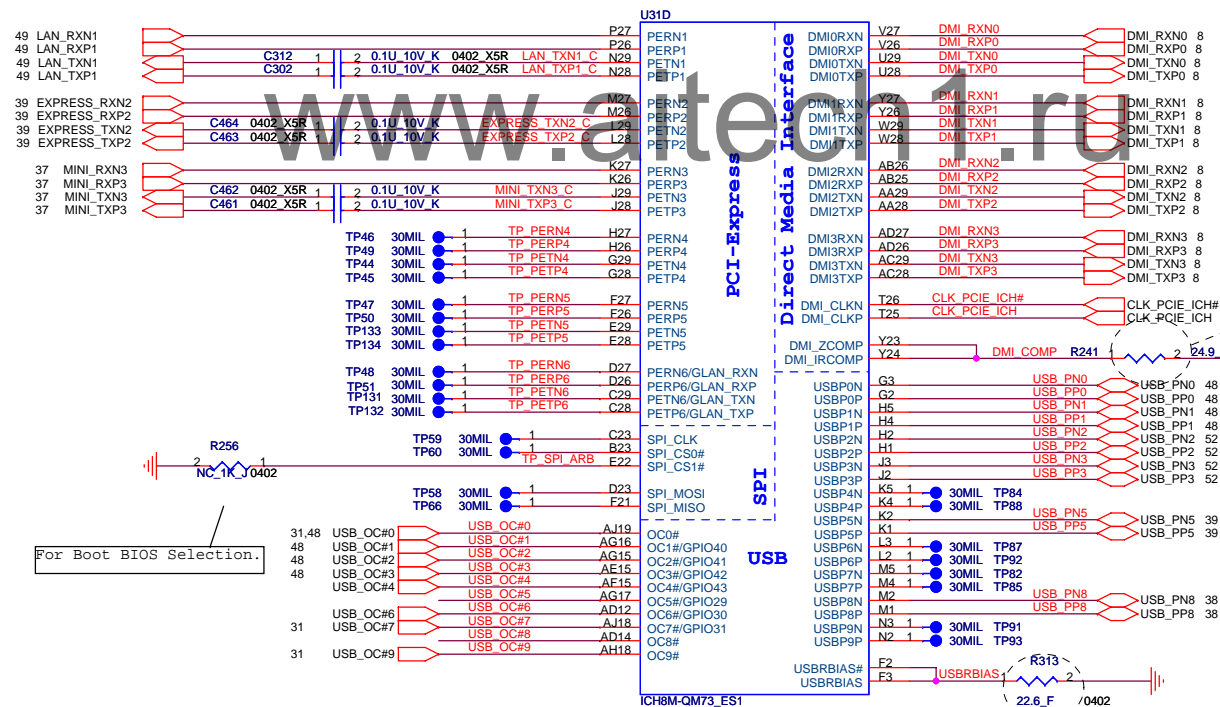




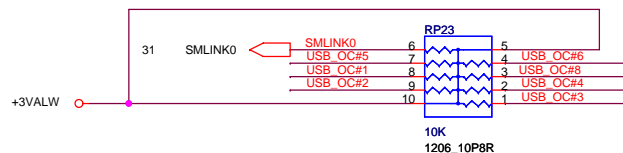
## PCI Pullups



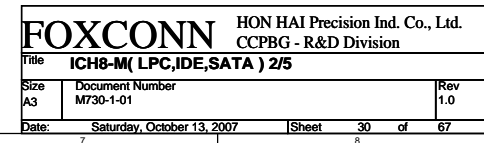
	GNT0#	SPI_CS
LPC(Default)	Hi	Hi
PCI	Hi	LOW
SPI	LOW	Hi

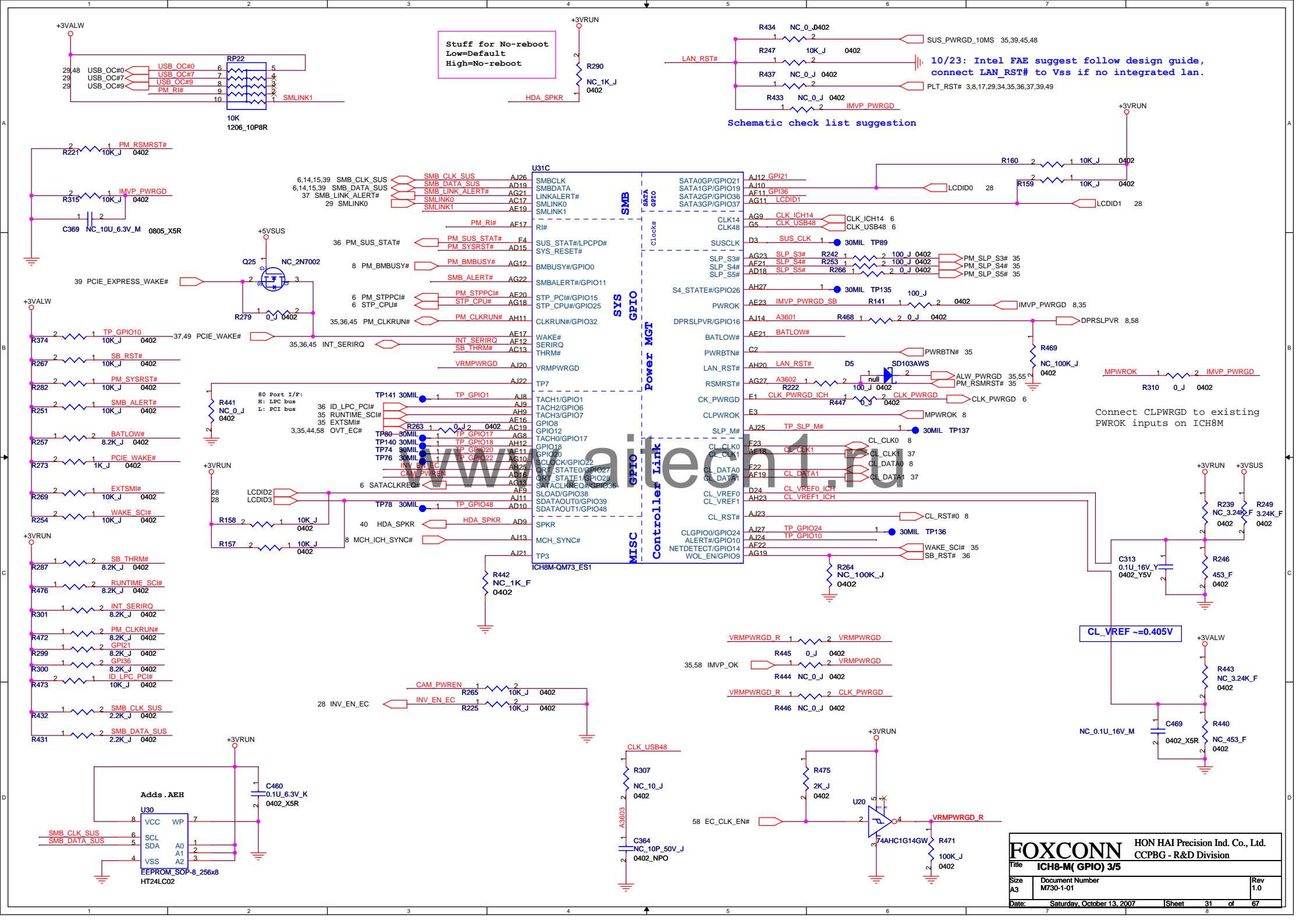


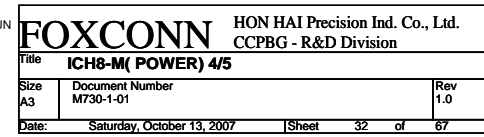
Place within  
500 mils of  
ICH

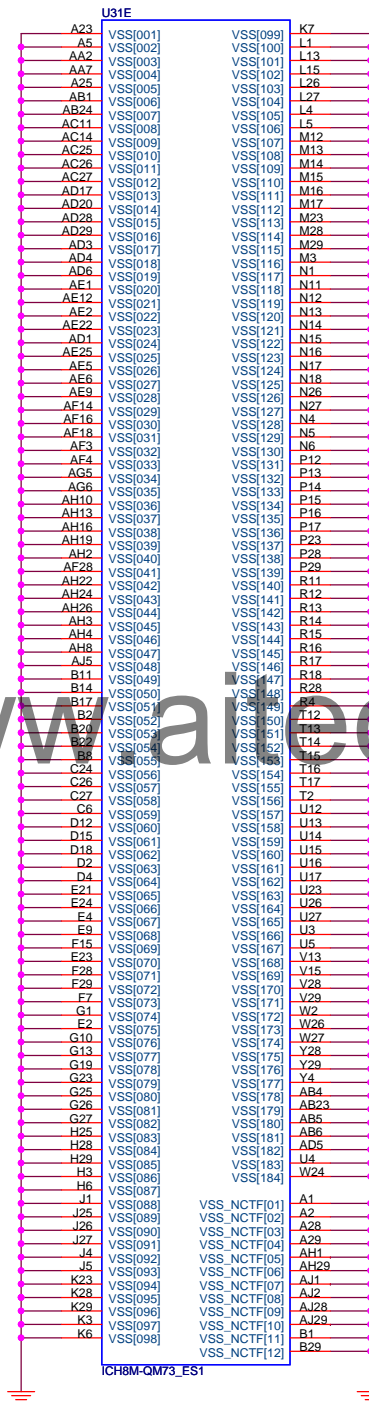


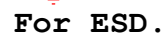
Place within 500 mils of  
ICH and don't routing next  
to high speed signals





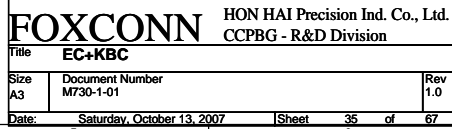


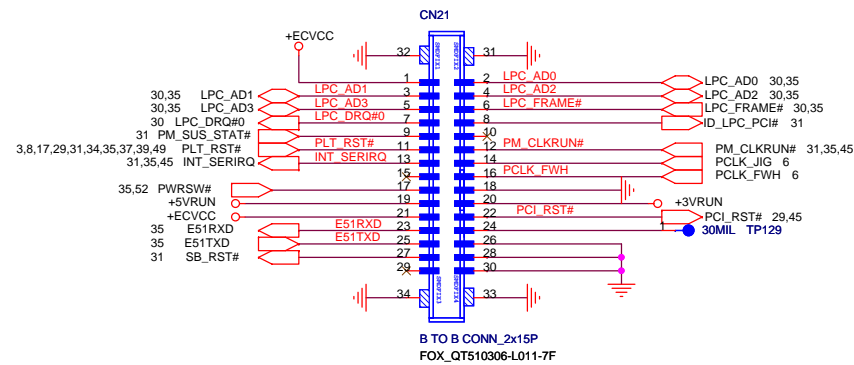
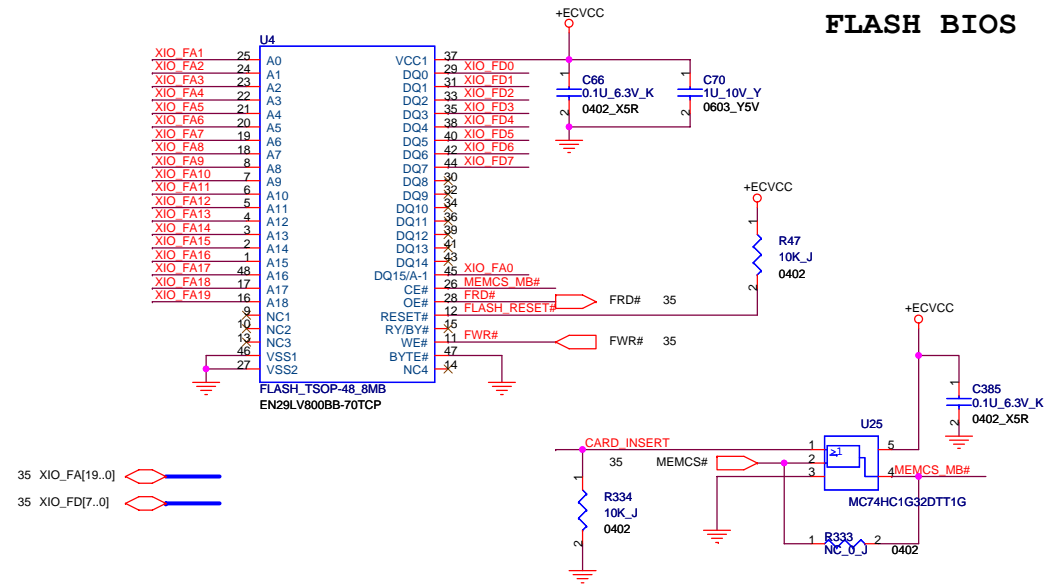




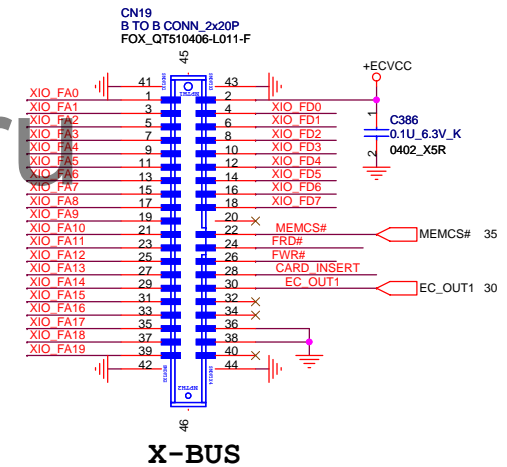
**CD-ROM CONN**







Pin 18 of JIG-120 is useless in debug board, so we let pin 18 NC.





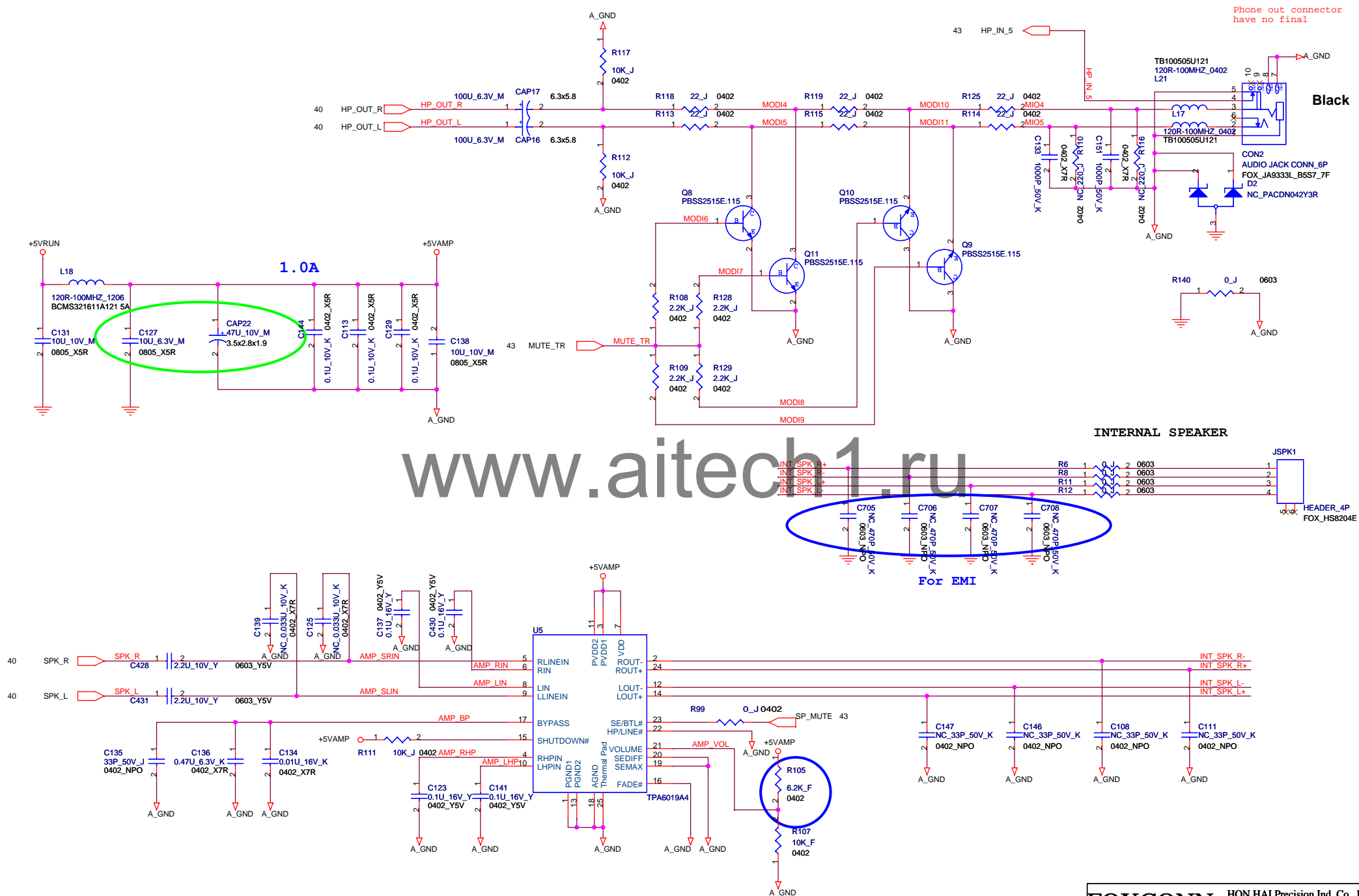


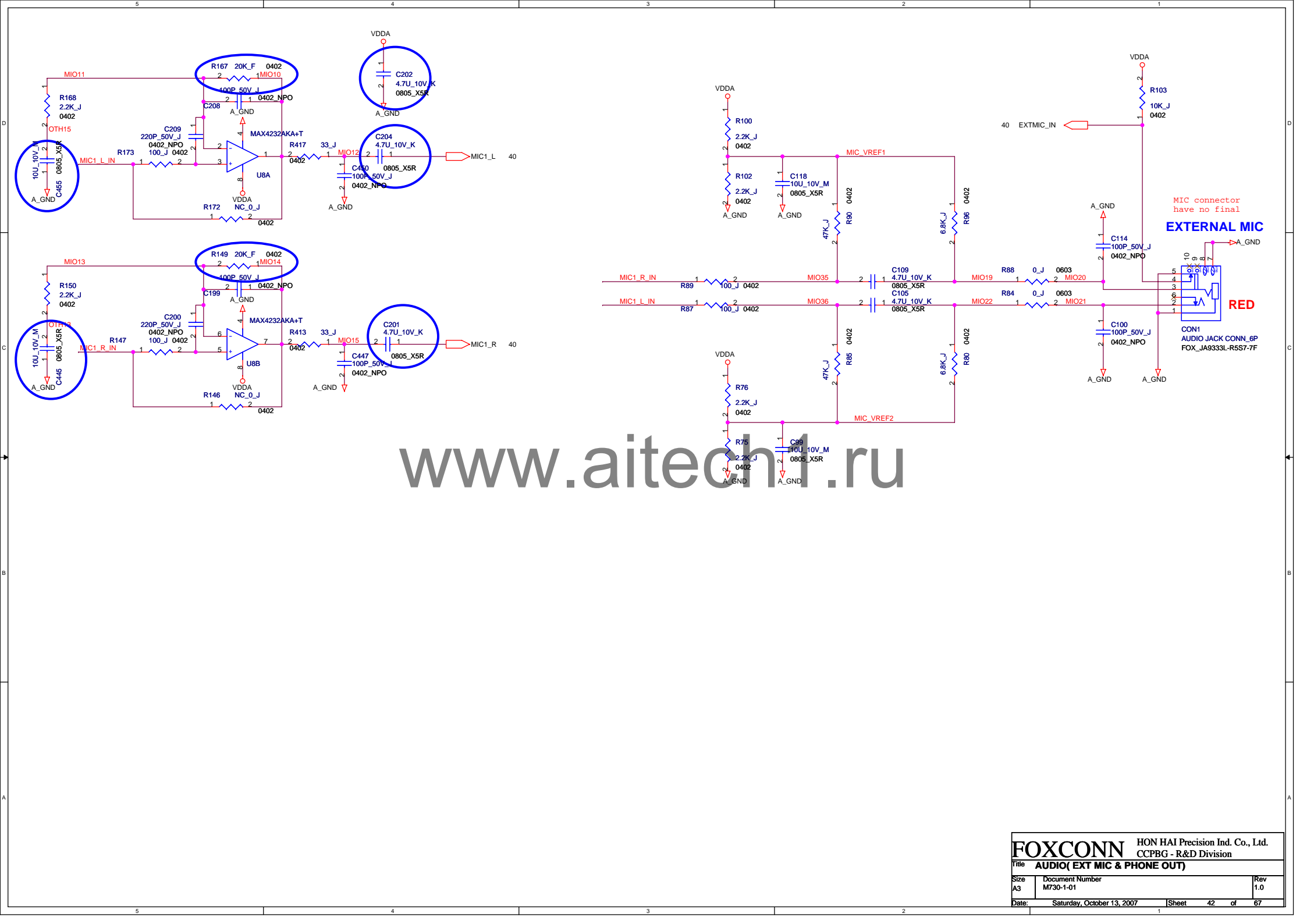




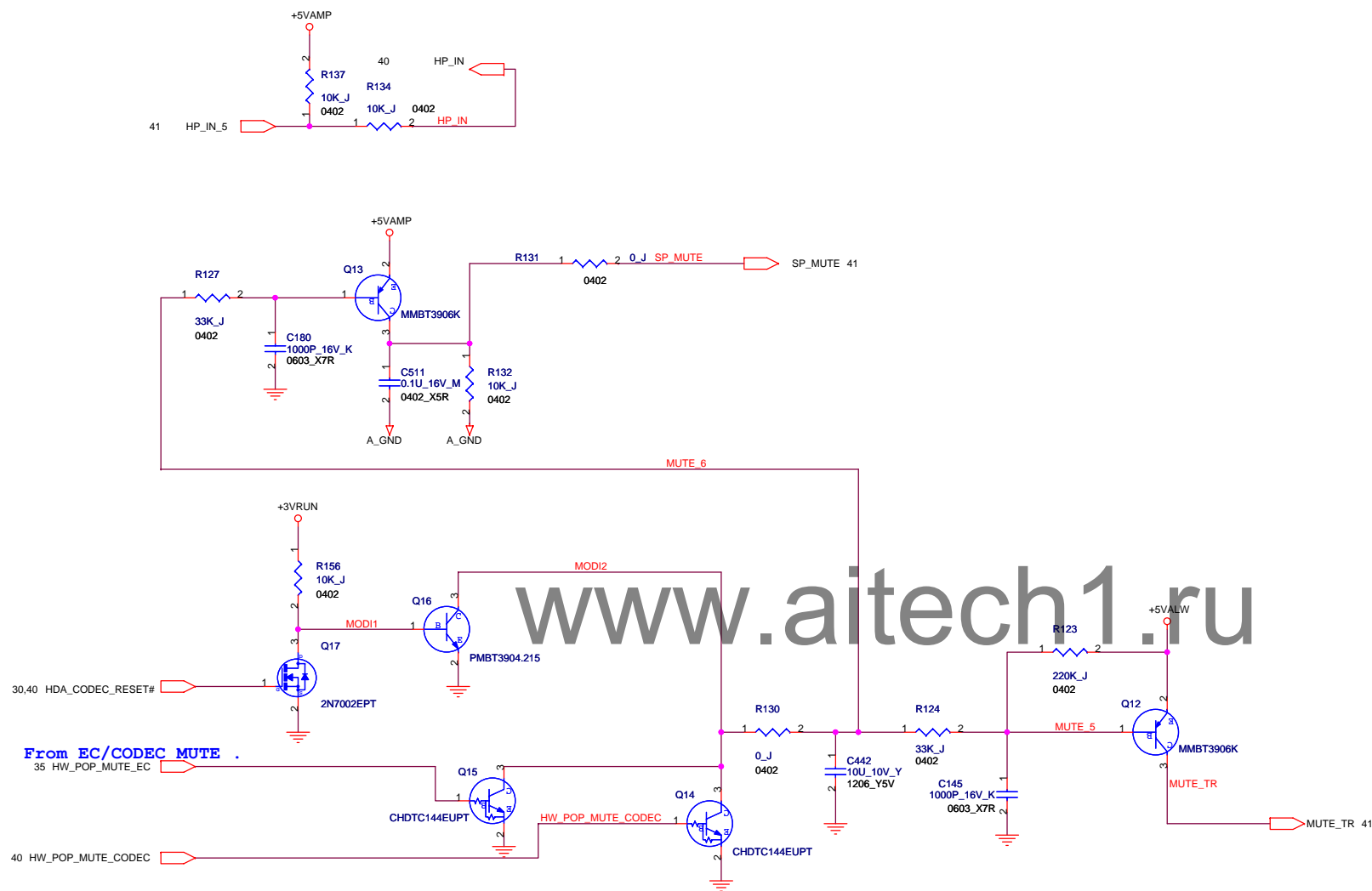


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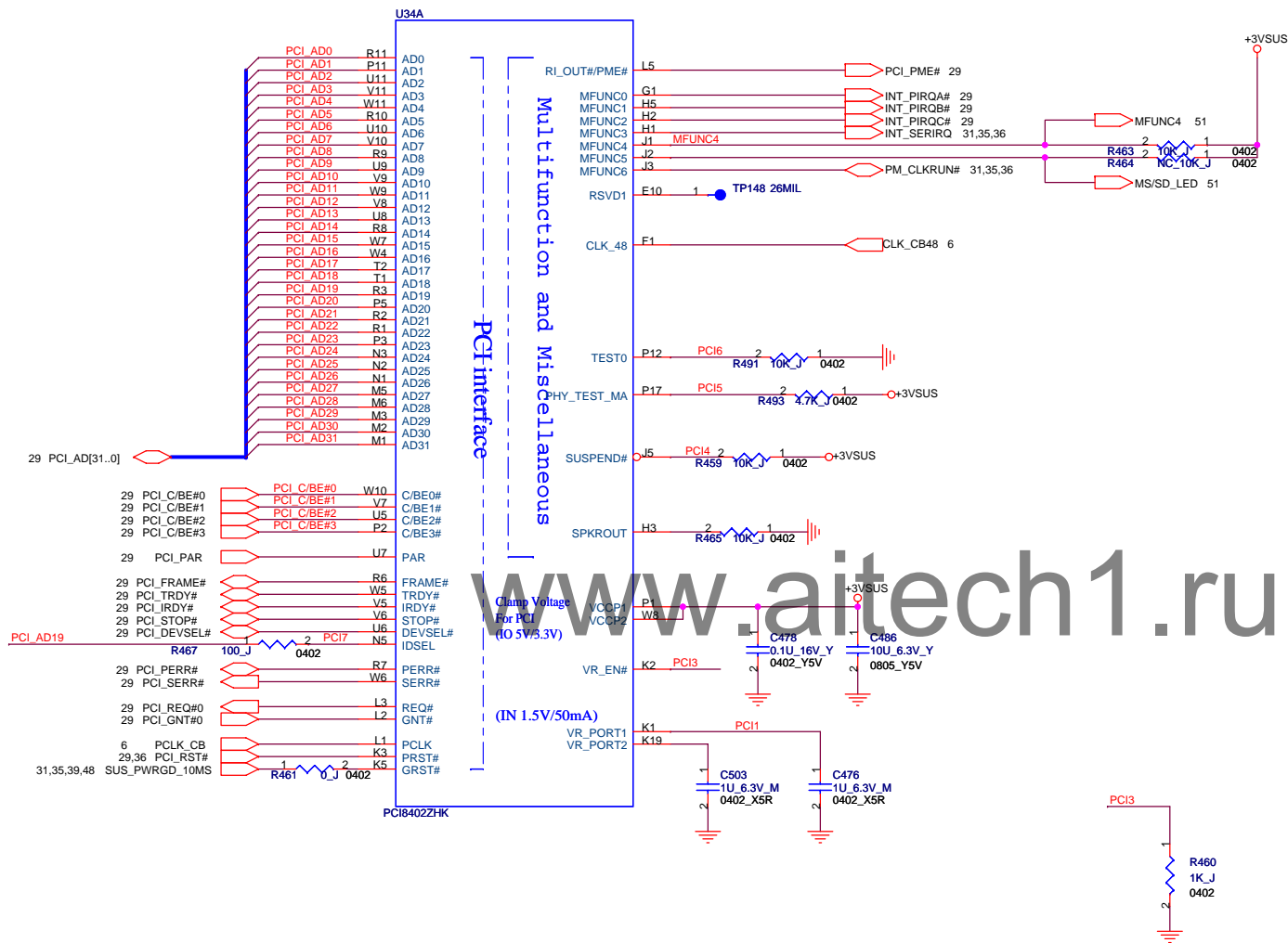


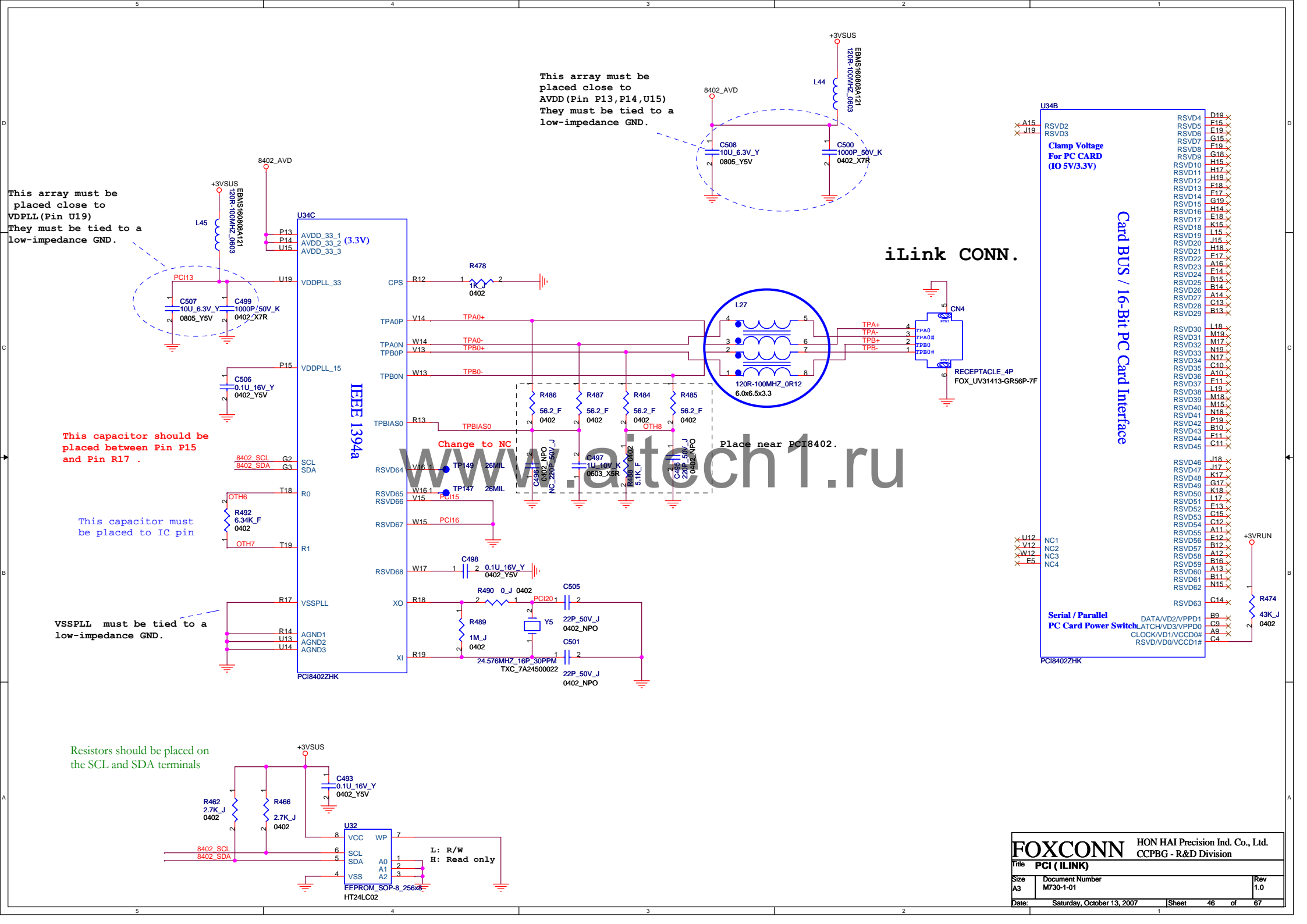




www.aitech1.ru

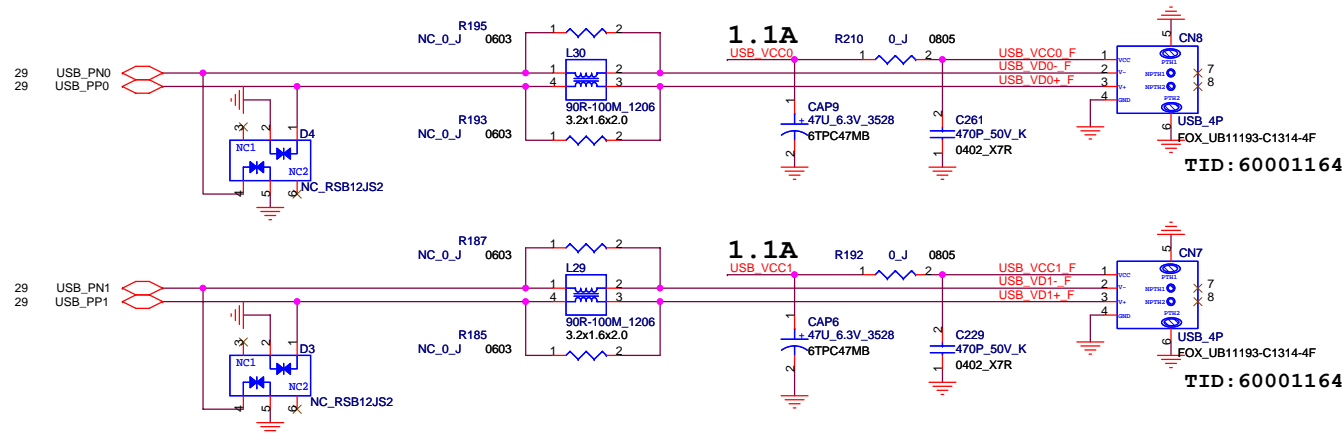




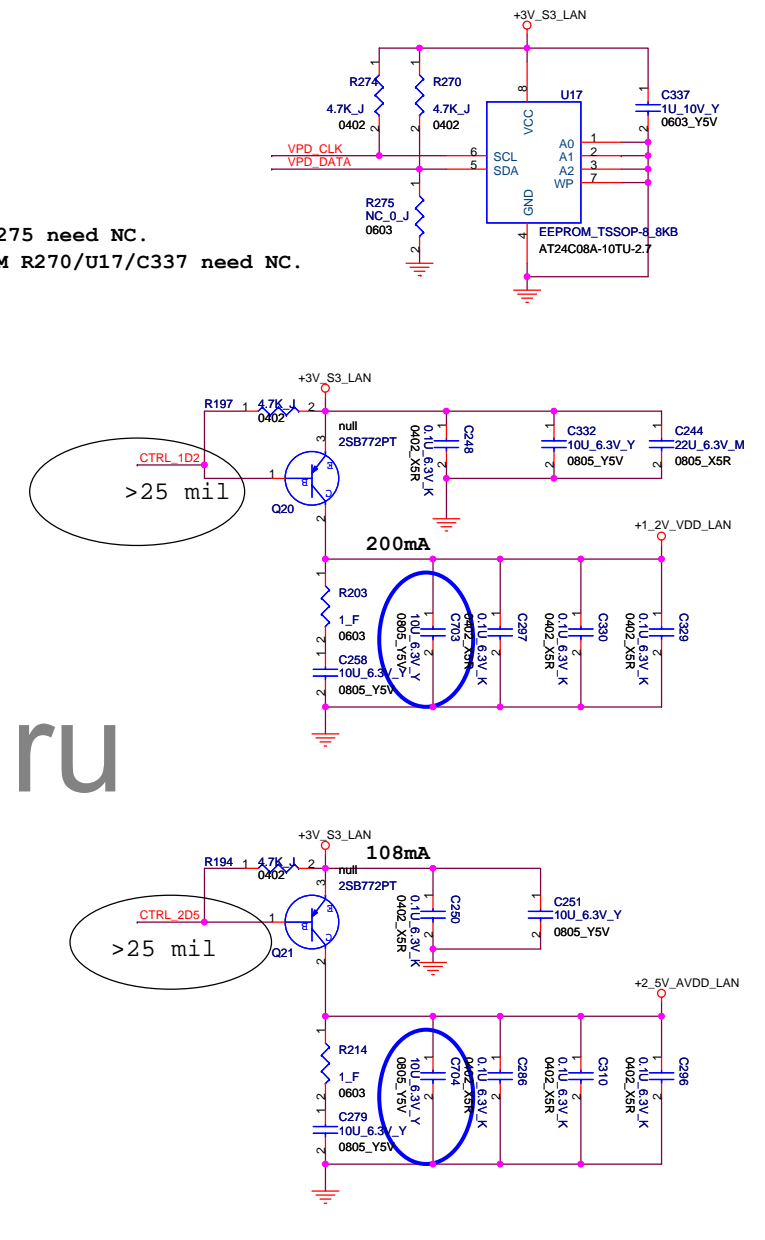




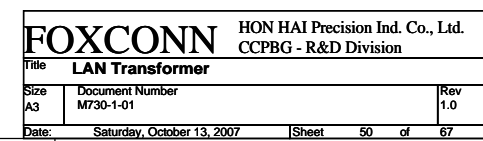
# USB CONN.



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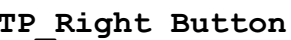
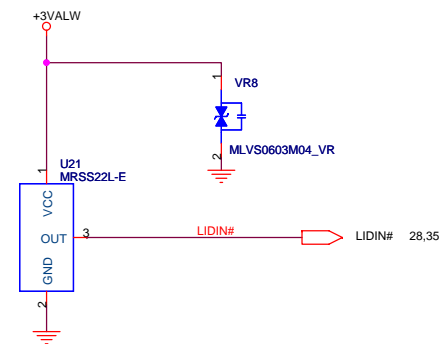
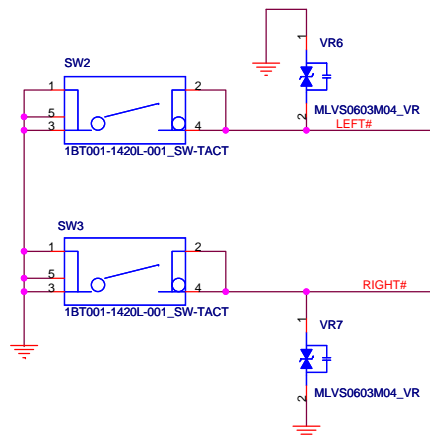
<b>FOXCONN</b>		<b>HON HAI PRECISION IND. CO., LTD.</b>	
Title		<b>CPBG - R&amp;D Division</b>	
<b>LAN (88E8036)</b>			
Size A3	Document Number <b>M730-1-01</b>	Rev <b>1.0</b>	
Date:	<b>Saturday, October 13, 2007</b>	Sheet	<b>49 of 67</b>





## TP LEFT Button

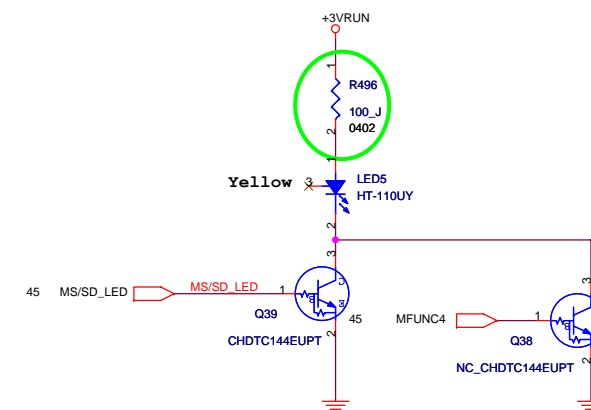
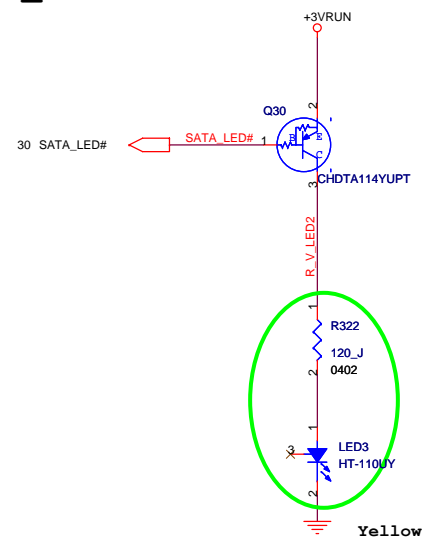
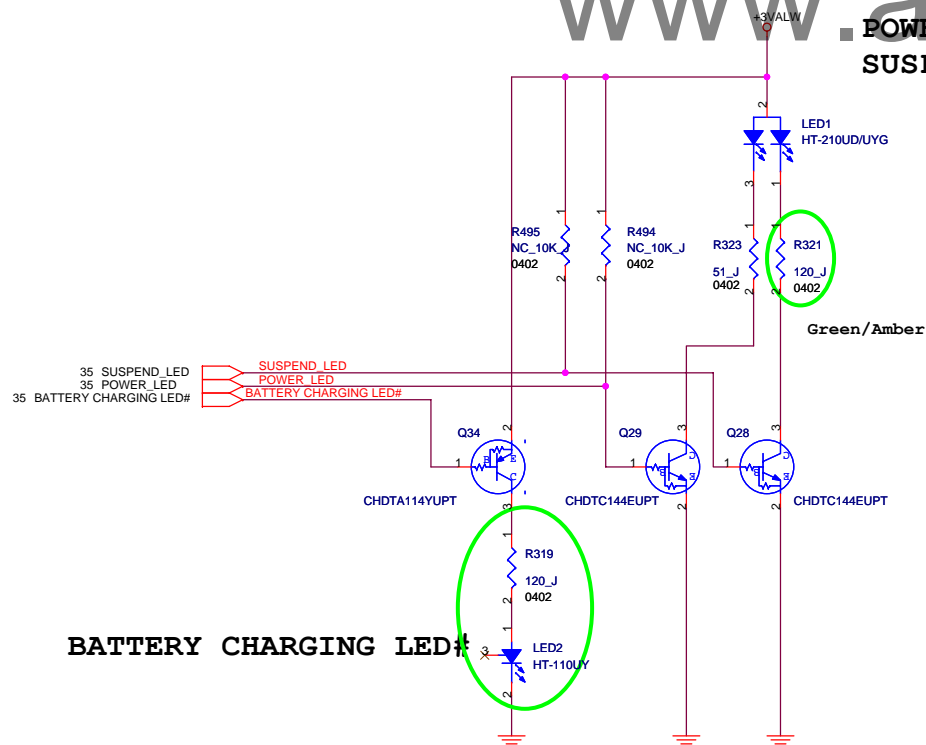
## TP\_Right Button



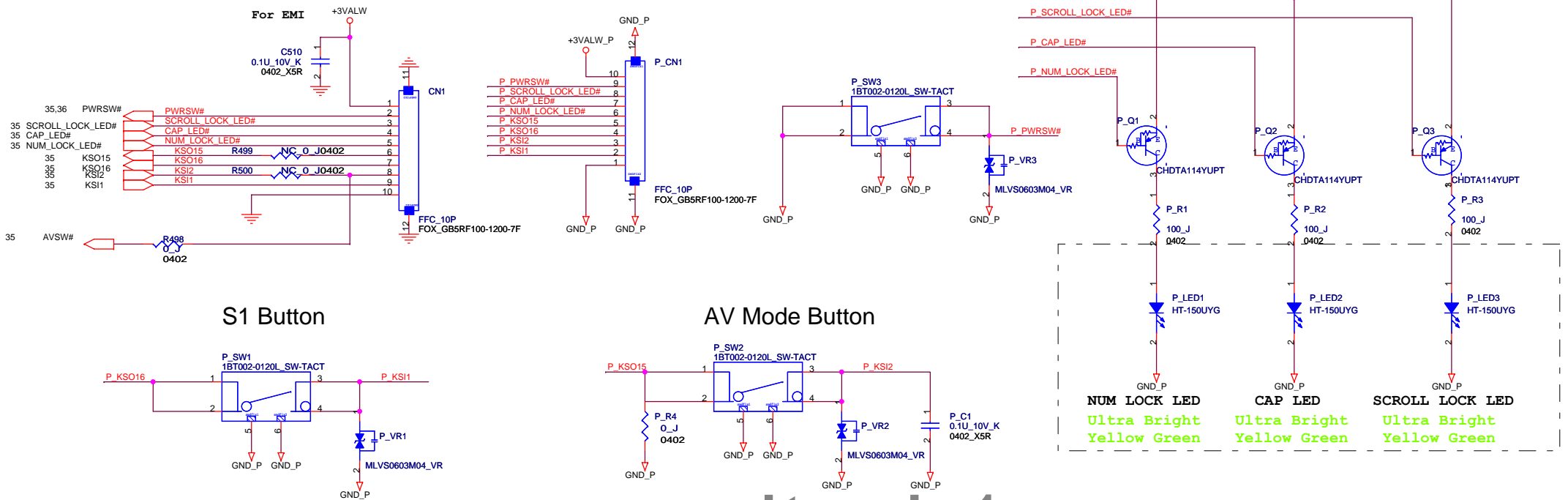
POWER\_LED  
SUSPEND\_LED

SATA LED#

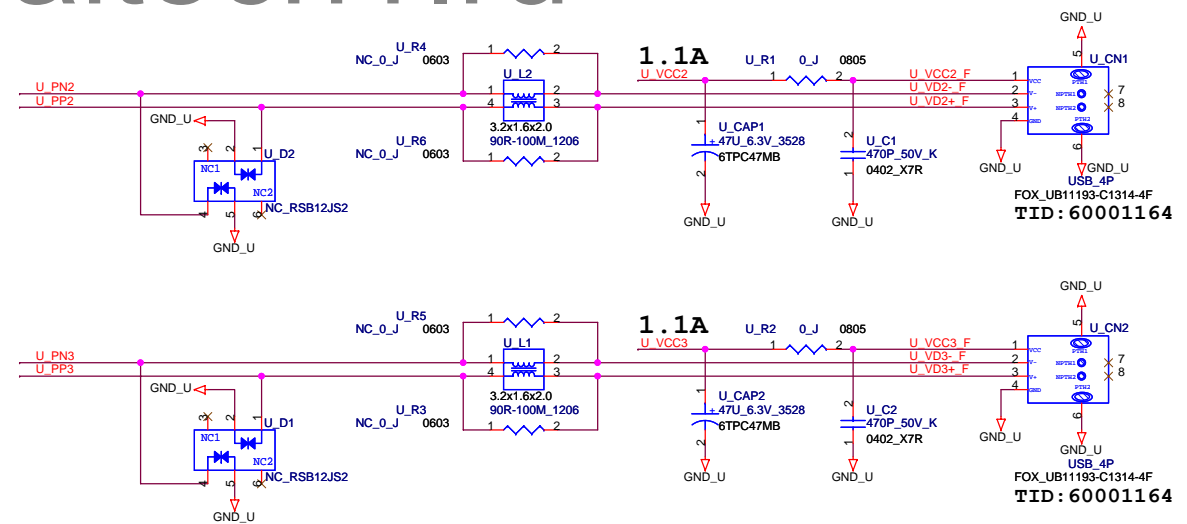
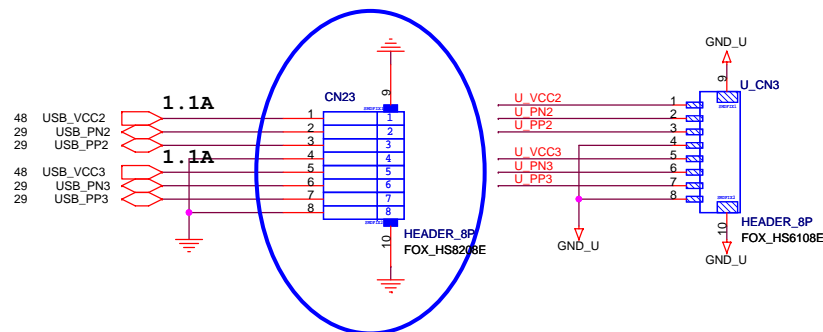
MS/SD LED

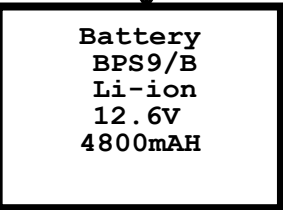
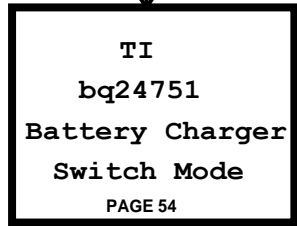


## Power Button Board



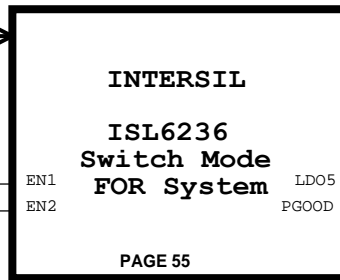
## USB Board





DCBATOUT

ALW\_ON



System

+5VALW/5.5A

System

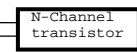
+3VALW/5A

+5VALW\_LDO

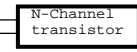
ALW\_PWRGD

+12V For Load switch

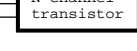
+5VALW\_LDO



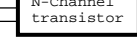
+5VSUS/1.6A



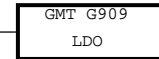
+5VRUN/3A



+3VSUS/1.6A



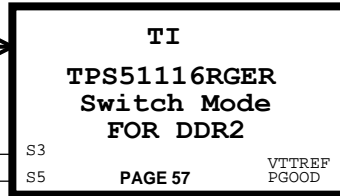
+3VRUN/3A



+ECVCC/100mA

DCBATOUT

SUS\_ON



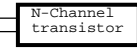
+1\_8VSUS/11A

+0\_9VSUS/2A

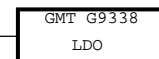
DDRDIMM\_VREF

DDR2\_PWRGD

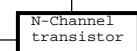
RUN\_ON2



+1\_8VRUN/6A



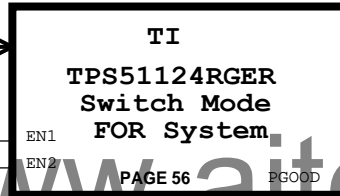
RUN\_ON



+1\_25RUN/1.7A

DCBATOUT

RUN\_ON

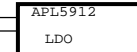


+1\_05VRUN/10A

+1\_5VRUN/6A

RUN\_PWRGD

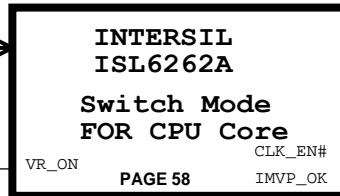
RUN\_ON1



PEX\_VDD/1.7A

DCBATOUT

IMVP\_VR\_ON



VHCORE/44A

CLK\_EN#

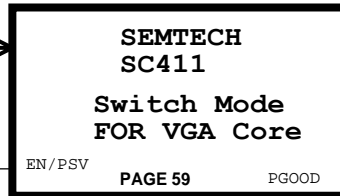
EC\_CLK\_EN#

IMVP\_OK

IMVP\_OK

DCBATOUT

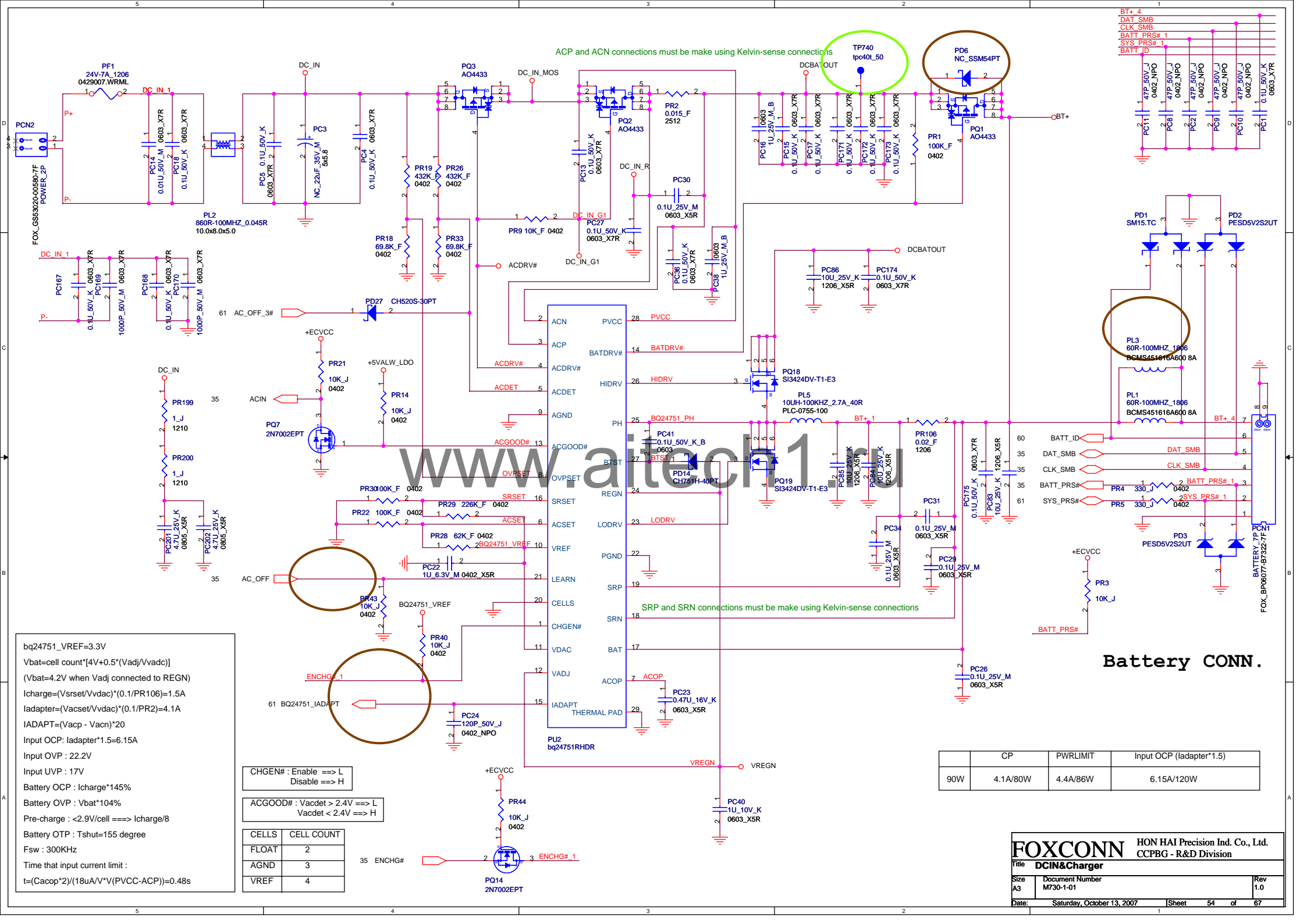
RUN\_ON1



NV\_VDD/12.5A

EN/PSV

PGOOD



ACP and ACN connections must be make using Kelvin-sense connections

TP740  
tpc40t\_50

PD6  
NC\_SSM54PT

BT+ 4  
DAT SMB  
CLK SMB  
BATT\_PR# 1  
SYS\_PR# 1  
BATT\_ID

PD1  
SM15.TC  
PD2  
PESD5V2S2UT

PL3  
60R-100MHZ\_1806  
BCMS451616A600 8A  
PL1  
60R-100MHZ\_1806  
BCMS451616A600 8A

### Battery CONN.

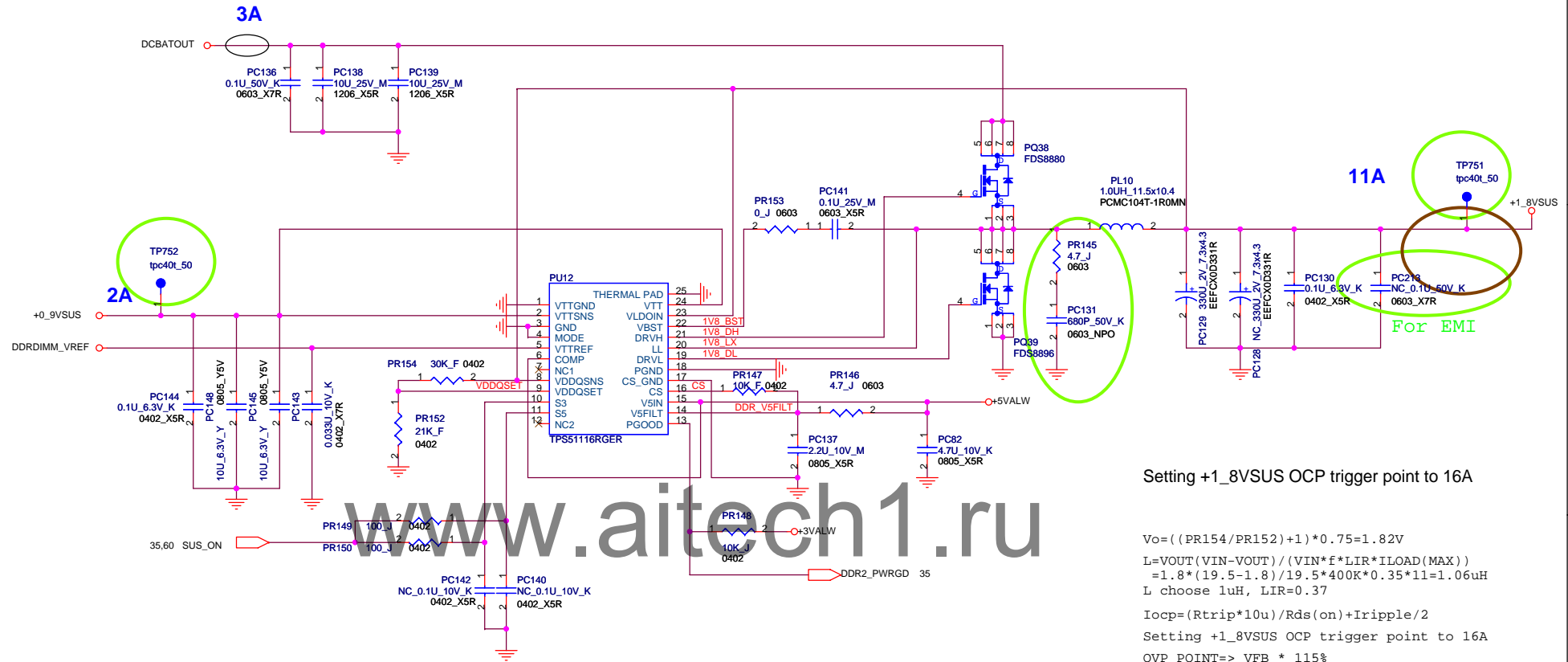
bq24751\_VREF=3.3V  
 $V_{bat} = \text{cell count} \times [4V + 0.5 \times (V_{adj}/V_{vdc})]$   
( $V_{bat} = 4.2V$  when  $V_{adj}$  connected to REGN)  
 $I_{charge} = (V_{srset}/V_{vdc}) \times (0.1/PR106) = 1.5A$   
 $I_{adapter} = (V_{acset}/V_{vdc}) \times (0.1/PR2) = 4.1A$   
 $I_{ADAPT} = (V_{acp} - V_{vacn}) \times 20$   
Input OCP:  $I_{adapter} \times 1.5 = 6.15A$   
Input OVP : 22.2V  
Input UVP : 17V  
Battery OCP :  $I_{charge} \times 145\%$   
Battery OVP :  $V_{bat} \times 104\%$   
Pre-charge :  $< 2.9V/\text{cell} \implies I_{charge}/8$   
Battery OTP :  $T_{shut} = 155 \text{ degree}$   
Fsw : 300KHz  
Time that input current limit :  
 $t = (C_{acop} \times 2) / (18uA/V \times (V_{VCC} - ACP)) = 0.48s$

CHGEN# : Enable ==> L Disable ==> H	
ACGOOD# : Vacdet > 2.4V ==> L Vacdet < 2.4V ==> H	
CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

	CP	PWRLIMIT	Input OCP (Iadapter*1.5)
90W	4.1A/80W	4.4A/86W	6.15A/120W







Setting +1.8VSUS OCP trigger point to 16A

$$V_o = ((PR154/PR152)+1)*0.75 = 1.82V$$

$$L = VOUT(VIN-VOUT) / (VIN*f*LIR*ILOAD(MAX))$$

$$= 1.8*(19.5-1.8) / (19.5*400K*0.35*11) = 1.06\mu H$$

$$L \text{ choose } 1\mu H, LIR=0.37$$

$$I_{ocp} = (R_{trip}*10u) / R_{ds(on)} + I_{ripple}/2$$

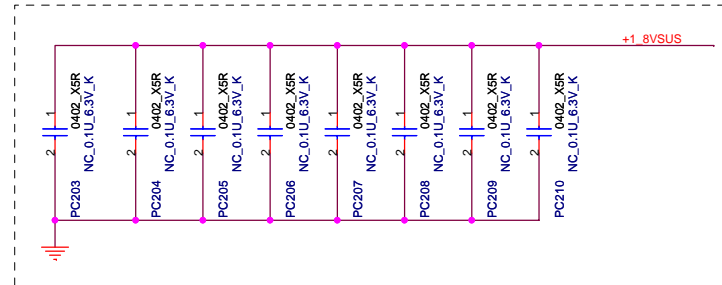
Setting +1.8VSUS OCP trigger point to 16A

OVP POINT=> VFB \* 115%

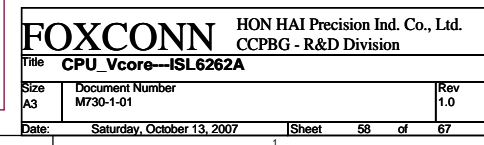
UVP POINT=> VFB \* 70%

Switching Frequency = 400KHz

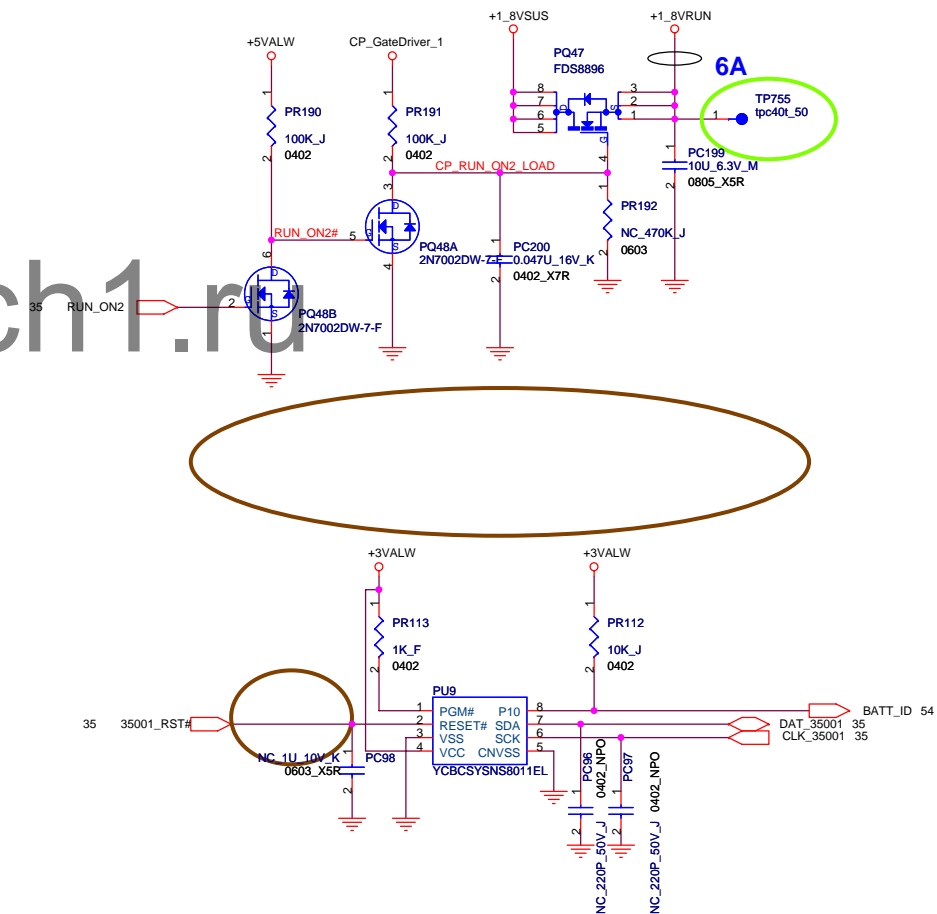
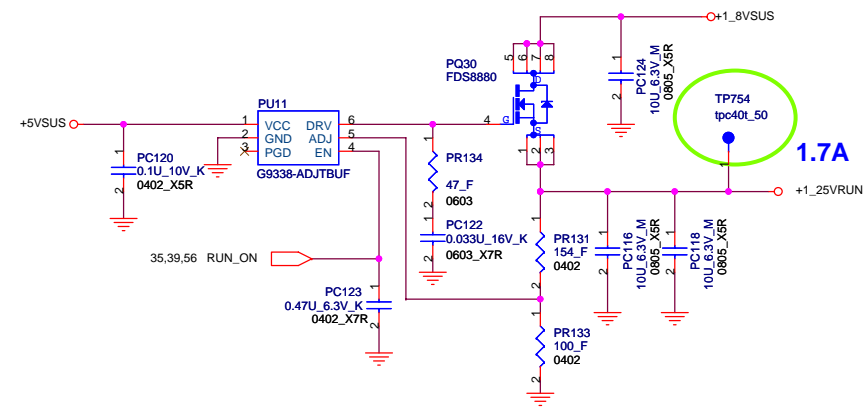
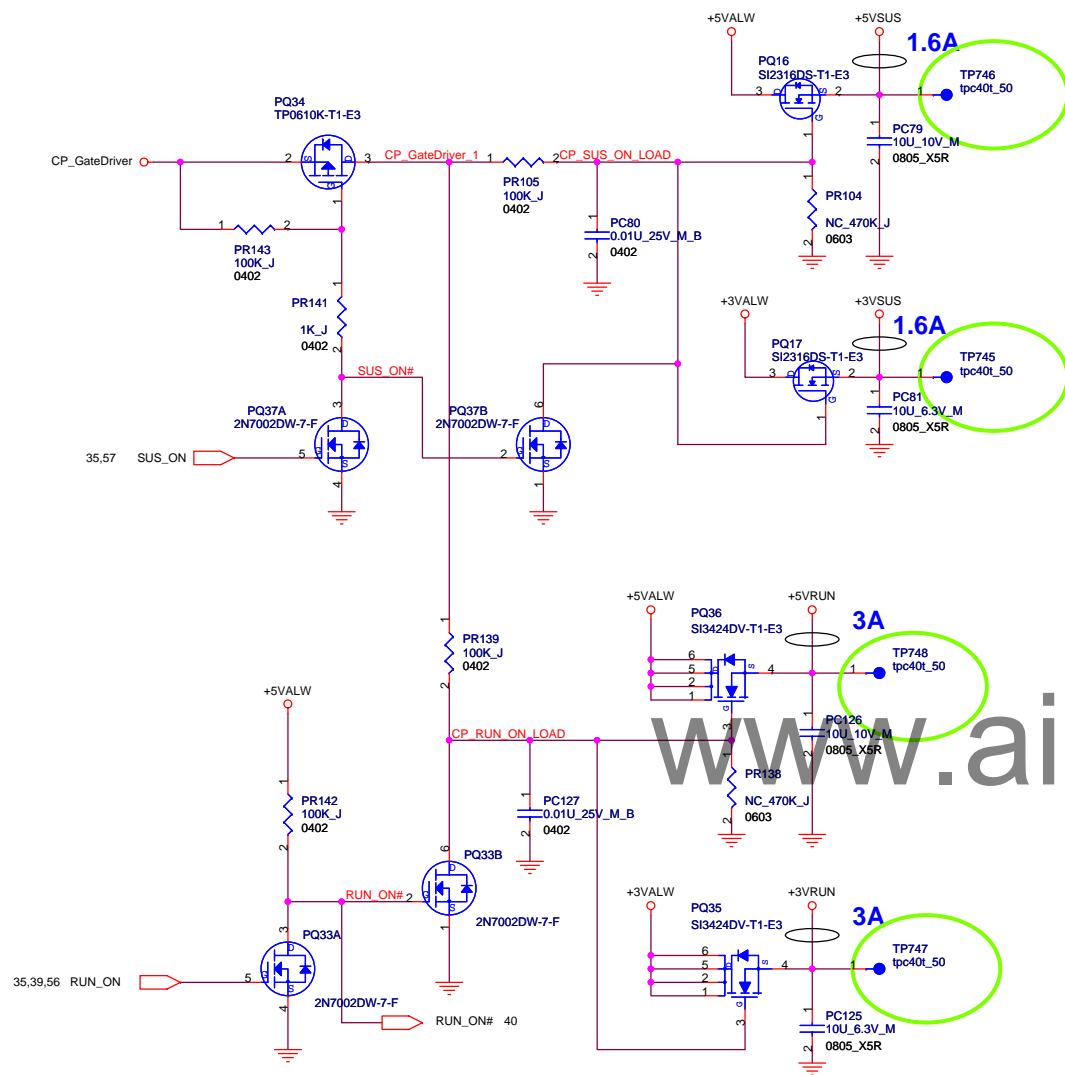
For EMI



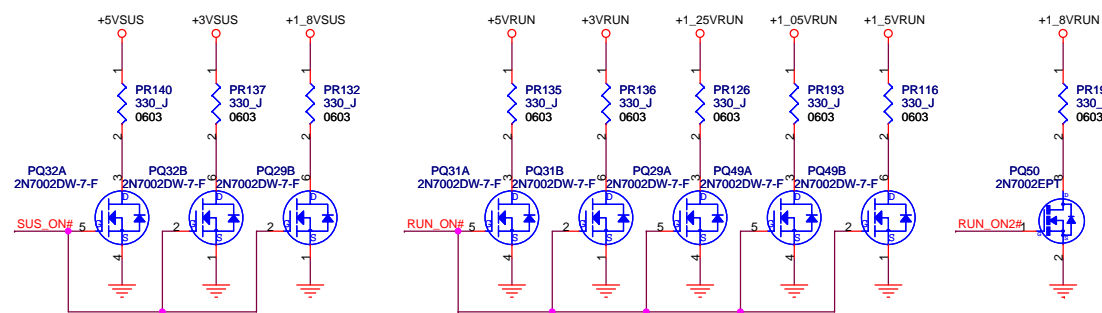




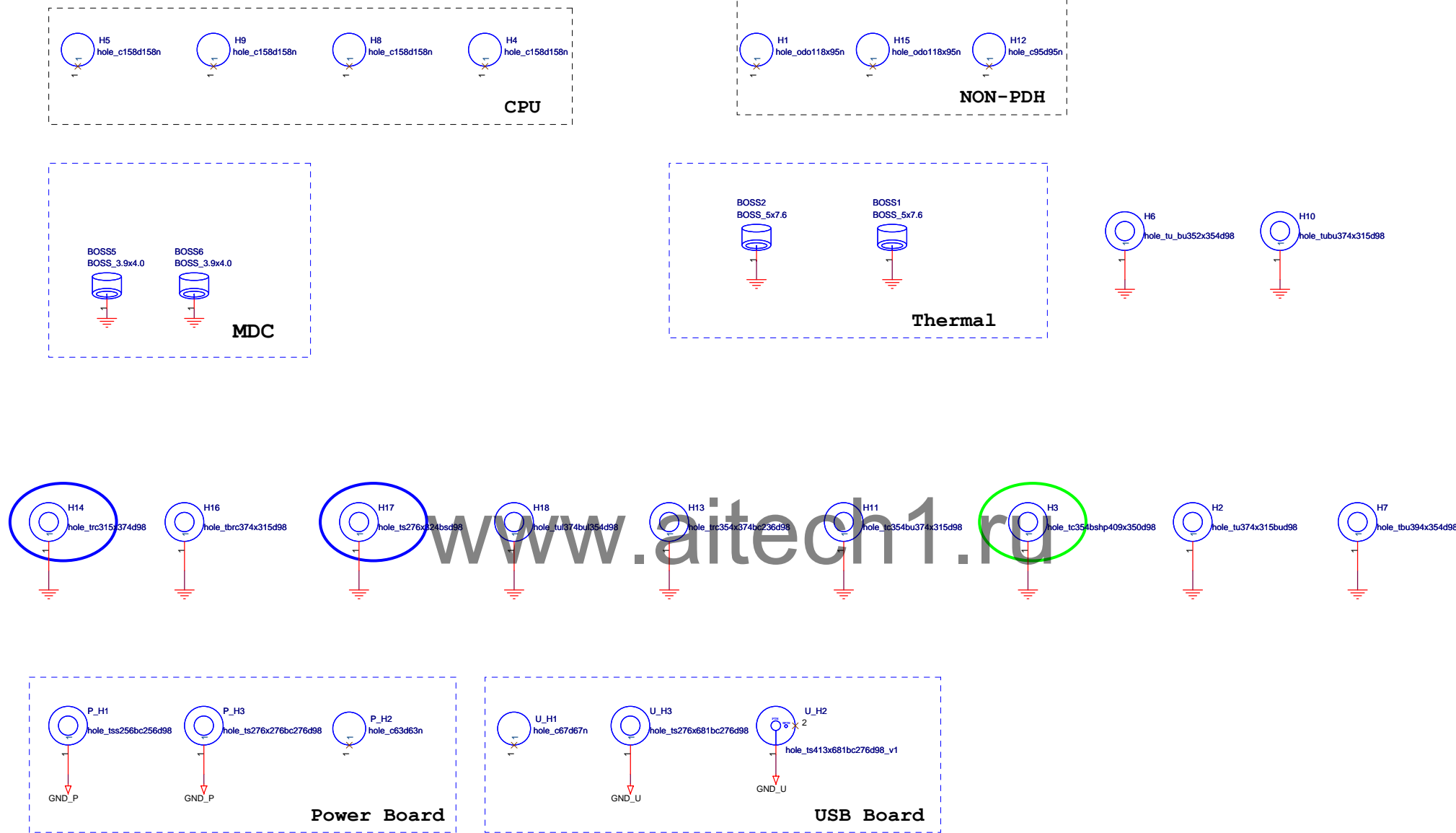




#### Discharge circuit for power-off







## M730 EVT

### (2007/05/29)

Base on M720\_SCHEMATIC\_0528\_1700.

### (2007/05/30)

P.35 Add R607 for OVT\_GFX#

P.23 Add R604,R605 and R606 for IFPC/D power

### (2007/05/31)

P.40 Change R171 to 22ohm,C215 to 22uf.

P.42 Change C201,C202,C204 to X5R.

P.44 Delete U12,R183,R190 and C224 for remove memory thermal sensor solution.

P.9 Delete R366,R69,R74 and R81.

P.11 Delete Internal graphics power.

P.12 Delete Internal graphics power.

P.54 Change PR2 from 0.02\_F 2512 to 0.015\_F 2512 for 90W adapter application.

P.60 Change PQ47 from SI4800BDY to FDS8896

P.28 Add C702

### (2007/06/04)

P.54 Change PR28 from 44.2K\_F to 62K\_F for setting constant power trigger point to 4.1A

P.57 Change PR147 from 6.8K\_F to 10K\_F for setting +1\_8VSUS OCP trigger point to 16A

P.59 Change PR184 from 14K\_F to 14.3K\_F for setting NV\_VDD to 1.215V

P.59 Change PR182 from 6.8K\_F to 5.9K\_F for setting NV\_VDD OCP to 18A

P.59 Add PR197, PR198 0\_J for NV\_VDD feedback remote sense.

P.61 Change PR56 from 53.6K\_F to 47K\_F for setting PWRLIMIT trigger point to 4.4A.

### (2007/06/05)

P.54 Change PQ18 and PQ19 from SI4800BDY to SI3424DV for layout space.

P.54 Change PC24 from 120pF 10% to 120pF 5% for purchase difficult.

P.60 Change PQ35 and PQ36 from SI4800BDY to SI3424DV for layout space.

### (2007/06/08)

P.62 Add BOSS7 and BOSS8 for thermal request

### (2007/06/14)

P.9 Change R97 to NC

P.9 Add R608/R609 and NC for LVDS\_VREFH and LVDS\_VREFL

P.8 Add TP731,TP732,TP733,TP734,TP735 for GFX\_VID[3:0] and GFX\_VR\_EN

### (2007/06/22)

P.19 Net I2CS\_SDA & I2CS\_SCL exchange with TP632 & TP633

P.22 Q40,Q41,Q42,Q43,R575,R576,R582 and R583 change from NC to mount for Nvidia save power function

P.24 Add and NC Q44,R610 for Nvidia save power function reserve

P.34 CAP7 change from 1C-41S0476-M000 to 1C-41R0476-M200 for layout convenient

P.62 Delete BOSS7,BOOS8 for ME request

### (2007/06/23)

P.62 H14 change to 1X-HOLE000-0474 for ME request

P.62 H17 change to 1X-HOLE000-0473 for ME request

### (2007/06/25)

P.62 Update H14 screw hole pad.

P.34 Change CAP7 to mount, and C275 to no mount for M720 HDD noise issue.

P.38 Update FeliCa pin define for M720 A'SSY issue.

P.49 Add C703,C704 for M720 LAN noise issue.

### (2007/06/28)

P.57 Delete PR151 0ohm for application note.

P.58 Change PC67 from 270pF 10% to 270pF 5% for purchase difficult.

P.58 Add TP736, TP737, TP738 and TP739 test pin for application note.

P.56 PL8 change from 1L-DSPD100-4H02 to 1T-00001U5-0000 for layout convenient.

### (2007/06/29)

P.22 Delete R569 and add R611 for mirror function off.

P.22 Modify address and command signals of U39 for mirror function off.

### (2007/07/02)

P.22 R577,R578,R573,R574 change from 4.3k to 1.05k for nVidia's suggestion.

P.22 R582,R583,R575,R576 change from 4.02k to 1.82k for nVidia's suggestion.

P.22 R584,R585,R579,R580 change from 10k to 2.49k for nVidia's suggestion.

P.28 Add R612 and NC R596,U40 for GPIO3 of GPU is active high which is nVidia's suggestion.

### (2007/07/03)

P.37 Change LED4 to HT-110YG for M720 LED issue.

P.51 Change R321,R323 to 51ohm,LED2,LED3 to HT-110Y for M720 LED issue.

P.48 Change F5~F8 to 2.6A poly-switch for M720 USB loading and noise issue.

P.52 Change CN23 to HS-8208E for M720 USB loading and noise issue.

### (2007/07/05)

P.11 L28 change to 1uH/220mA for M720 component spec. issue.

P.08 Delete C509 for layout convenient.

P.46 Change L27 to SINKA OD6560T-E900T for purchase difficult.

P.28 NC R612 and mount R596,U40 for GPIO3 of GPU is set active low which is the same as MS90.

P.22 Swap data signals of VRAM for layout convenient.

### (2007/07/06)

P.54 Change PC3 from mount to dummy for M720 application note.

P.54 Change PC38 from 4.7uF\_25V 0805 to 1uF\_25V 0603 for M720 application note.

P.54 Remove PR176 10\_J for M720 application note.

P.54 Add PR199, PR200 1\_J 1206 and PC201, PC202 4.7uF\_25V 0805 for M720 DC\_IN RC snubber circuit.

P.38 L25 change from BK1608LL121-T to TB160808B121 for purchase difficult.

P.54 PL1,PL3 change from BLM41PG600SN1L to BCMS451616A600-8A for purchase difficult.

P.05 CAP3 change from EEFSLOD331EY to 2R5TPE330M9 for purchase difficult.

P.12 CAP14 change from EEFSLOD331EY to 2R5TPE330M9 for purchase difficult.

### (2007/07/09)

P.54 Change PR199, PR200 form 1206 to 1210 for M720 power rating safety.

P.05 CAP3 change back to EEFSLOD331EY for purchase difficult.

P.12 CAP14 change back to EEFSLOD331EY for purchase difficult.

### (2007/07/10)

P.11 L28 change to EBLS2012-1R0M 0.25A for M720 component spec. issue.

### (2007/07/11)

P.28 Add L55 for M720 EMI issue.

P.41 Delete VR2~VR5 and add C705~C708(NC) for M720 EMI issue.

FOXCONN			HON HAI Precision Ind. Co., Ltd.	
Title			CCPBG - R&D Division	
History (1)				
Size	Document Number		Rev	
A3	M730-1-01		1.0	
Date:	Saturday, October 13, 2007		Sheet	63 of 67

(2007/07/12)  
P.54 Add PJ9 for application.  
P.55 PR170,PR171,PC178,PC179 change to NC for application.  
P.59 PR183,PC189 change to NC for application.  
P.22 Change Q40~Q43 and R575,R576,R582,R583 to NC for customer request.  
P.06 Add C709,C710 and reserve for EMI application.  
P.57 Add PC203~PC210 and reserve for EMI application.  
P.35 Add C711,C712 and reserve for EMI application.  
P.38 Add C713 and reserve for EMI application.

(2007/07/13)  
P.40 Add J2 for EMI application.

(2007/07/16)  
P.42 Change C455,C445 to 10uF,R167,R149 to 20 Kohm for M720 MIC. THD+N issue.  
P.35 Change R382 to mount and R390 to NC for system ID modification.  
P.54 PR199,PR200 change to 1/3 W for PUR issue.

(2007/07/17)  
P.37 Change LED4 to HT-110UYG for M720 MOR request.

(2007/07/20)  
P.41 Change R105 to 6.2Kohm for M720 audio issue.

M730 DVT

(2007/07/27)  
P.48 Delete F6,F8 for MOR's request.  
P.61 Change PD16 from mount to NC, add PR201 0ohm for application.  
P.06 Modify R350 pin1 connection from GND to +3VRUN for GPU select 27MHz issue.

(2007/08/13)  
P.51 Change LED2,LED3 from HT-110Y to HT-110UY  
Change R319,R322 from 47ohm to 120ohm and R321 from 51ohm to 120ohm  
Change R496 from 47ohm to 100ohm for M720 LED brightness request from MOR

(2007/08/14)  
Add test pin TP740~TP772 for power test jig.

(2007/08/17)  
P.34 Add CAP21 for +5VRUN noise issue of ODD  
P.41 Add CAP22 for +5VAMP noise issue of CODEC  
C127 change from no mount to mount for +5VAMP noise issue of CODEC  
P.25 Add C714/C715 for PEX\_PLL\_AVDD/PEX\_PLL\_DVDD noise issue

(2007/08/23)  
P.38 NC R152,R151,F2,L25,C185,C186,CN6 for no Felica SKU  
P.44 U27 change from GMT G781-1P8f to SMSC EMC1402-2-ACZL for Penryn CPU concern

(2007/08/25)  
P.62 H3 change to 1X-HOLE000-0519 for ME's request

(2007/08/28)  
P.55 PL11,PL12 change from SPD1004HT4R7N-8A to PCMC063T-4R7MN  
for ME interference issue.  
P.55 PR170,PR171,PC178,PC179 change from NC to mount for EMI issue.  
P.57 PR145 change from 3.3ohm to 4.7ohm and PC131 change from 1000P to 680P  
for EMI issue.

(2007/08/28)  
P.35 Add and reserve C716,C717,C718 0603 cap for EMI solution.  
P.55 Add and reserve PC211,PC212 0603 cap for EMI solution.  
P.57 Add and reserve PC213 0603 cap for EMI solution.  
P.58 Add and reserve PC214~PC218 0603 cap for EMI solution.

M730 PVT

(2007/09/27)  
P.54 Delete PJ9 for application.  
P.54 Change PD6 from mount to NC for UL\_Lock issue.  
P.54 Delete PR25, PR41, PR42 for application.  
P.55 PL11,PL12 change from PCMC063T-4R7MN to SPD1004HT4R7N-8A  
for MOR request.  
P.55 Delete PJ4, PJ5 for application.  
P.55 Delete PR155, PR156, PR162, PR163, PR167 for application.  
P.56 Delete PJ1, PJ2 for application.  
P.56 Delete PR129 for application.  
P.57 Delete PJ3 for application.  
P.58 Delete PR70, PR71, PR84, PR86, PR90, PR93, PR94, PR96, PR97, PR99,  
PR102 for application.  
P.59 Delete PJ6, PJ7 for application.  
P.59 Delete PR177, PR197, PR198 for application.  
P.60 Delete PR110, PR111, PR114 for application.  
P.61 Delete PR20, PR49 for application.

(2007/10/17)  
P.25 Add netname "J6" for U35 Pin J6 for application.

(2007/10/19)  
P.47 Change R235 from 47ohm to 68ohm for MS Card Media-C  
MS\_CLK undershoot issue

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	<b>History ( 2 )</b>		
Size	Document Number	Rev	
A3	M730-1-01	1.0	
Date:	Friday, October 19, 2007	Sheet	64 of 67



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<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	<b>History ( 3 )</b>		
Size A3	Document Number M730-1-01	Rev 1.0	
Date:	Saturday, October 13, 2007	Sheet	65 of 67

www.aitech1.ru

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <b>History (4)</b>			
Size A3	Document Number M730-1-01		Rev 1.0
Date:	Saturday, October 13, 2007	Sheet 66 of 67	

www.aitech1.ru

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <b>History ( 5 )</b>			
Size A3	Document Number M730-1-01		Rev 1.0
Date:	Saturday, October 13, 2007	Sheet 67 of	67